



GX04828 Ultra Low-Noise Clock Jitter Cleaner

FEATURES

- JEDEC JESD204B Support
- Ultra-Low RMS Jitter
 - 104fs RMS Jitter (10kHz to 20MHz)
 - 161dBc/Hz Noise Floor at 245.76 MHz
- Up to 14 Differential Device Clocks from PLL2
 - Up to 7 SYSREF Clocks
 - Maximum Clock Output Frequency 3.1 GHz
 - LVPECL, LVDS, HSDS, LCPECL
 - Programmable Outputs from PLL2
- Up to 1 Buffered VCXO/Crystal Output from PLL1
 - LVPECL, LVDS, 2xLVCMOS Programmable
- PLL1
 - Up to 3 Redundant Input Clocks
 - Automatic and Manual Switch-Over Modes
 - Hitless Switching and LOS
 - Integrated Low-Noise Crystal Oscillator Circuit
 - Holdover Mode When Input Clocks are Lost
- PLL2
 - Phase Detector Rate up to 155 MHz
 - Two Integrated Low-Noise VCOs
- 50% Duty Cycle Output Divides, 1 to 32 (even and odd)
- Precision Digital Delay, Dynamically Adjustable
- 23 ps Step Analog Delay
- Multi-Mode: Dual PLL, Single PLL, and Clock Distribution
- Industrial Temperature Range: -40 to 85°C
- 3.15V to 3.45V Operation
- Package: 64-Pin QFN

APPLICATIONS

- Wireless Infrastructure
- Data Converter Clocking
- Networking, SONET/SDH, DSLAM
- Medical / Video
- Measurement

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FUNCTIONAL BLOCK DIAGRAM

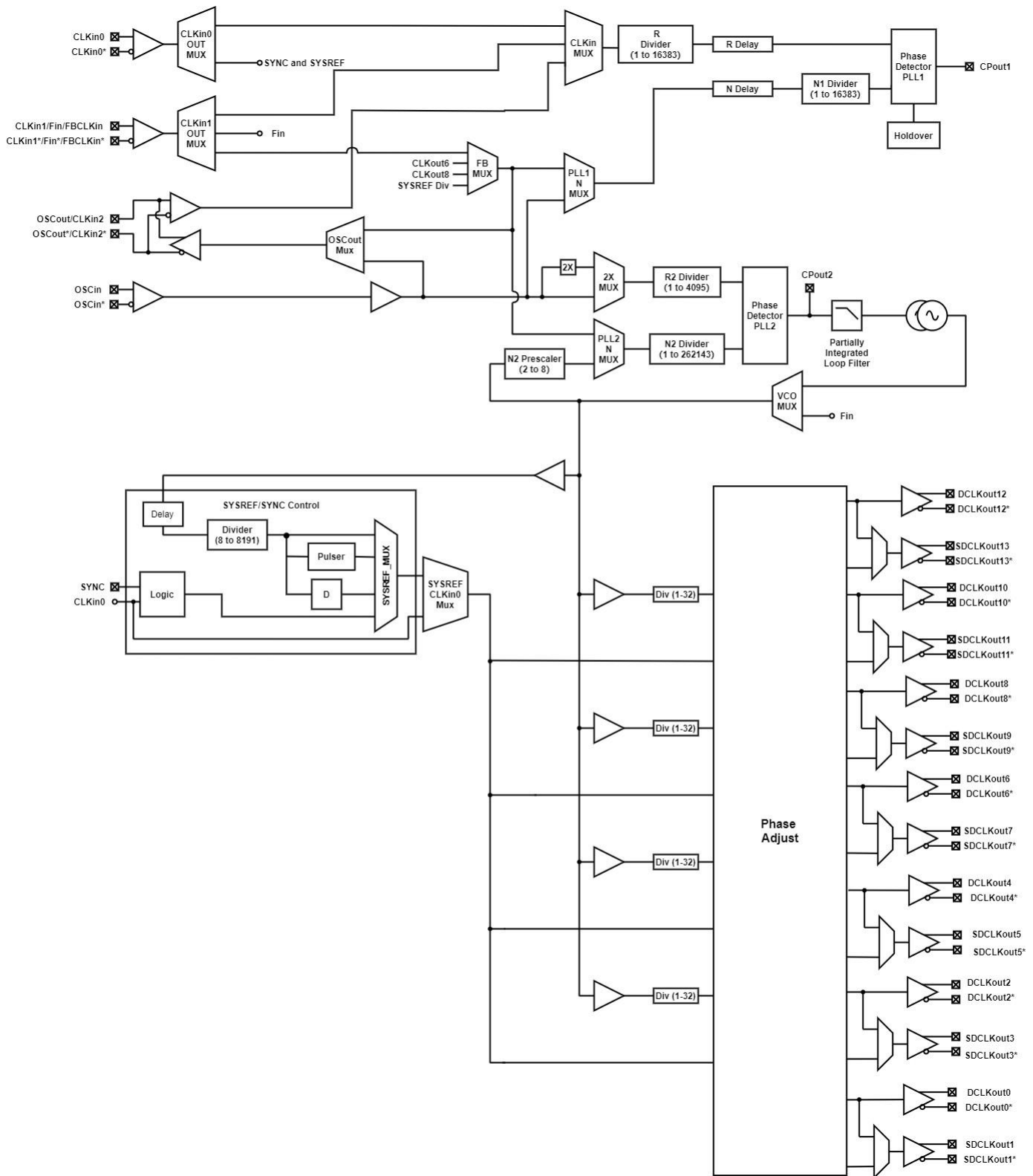


Figure 1 Functional Block Diagram



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DESCRIPTION

The GX04828 is a high performance clock conditioner with JEDEC JESD204B support. The 14 clock outputs from PLL2 can be configured to drive seven JESD204B converters or other logic devices, using device and SYSREF clocks. SYSREF can be provided using both DC and AC coupling. Not limited to JESD204B applications, each of the 14 outputs can be individually configured as high performance outputs for traditional clocking systems.

The high performance, low-power consumption, dual VCOs, dynamic digital delay, signal loss hold, make the GX04828 ideal for providing flexible high performance clocking trees.



ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	-0.3V to 3.6V
Input Signal Voltage V_{IN}	-0.3V to $V_{CC} + 0.3V$
Current $I_{IN}(\text{CLKin}/X/X^*, \text{OSCin}/\text{OSCin}^*, \text{FBCLKin}/in^*, \text{Fin}/\text{Fin}^*)$	$\pm 5\text{mA}$
Pin Temperature (soldering 4s)	260°C
Maximum Junction Temperature $T_{J,MAX}$	150°C
Operating Temperature Range	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
ESD(Human Body Model).....	$\pm 2000\text{V}$
ESD(Charged Device Model).....	$\pm 500\text{V}$

ATTENTION: Working above these ratings may cause permanent damage. In practice, do not operate the device at or above this limit.



ESD CAUTION

This product is an electrostatic sensitive device. When holding it, take appropriate ESD protection measures to avoid performance degradation or functional failure.

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TECHNICAL SPECIFICATIONS

Recommended Operation Conditions

Table 1 Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNIT
Junction temperature T_j			125	°C
Operating temperature	-40	25	85	°C
Supply voltage V_{CC}	3.15	3.3	3.45	V

Electrical Characteristics

3.15 V < V_{CC} < 3.45 V, -40 °C < T_A < 85 °C. Typical values at V_{CC} = 3.3 V, T_A = 25 °C, unless otherwise specified.

Table 2 Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
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CURRENT CONSUMPTION

Power down supply current (I_{CC_PD})			1.5		mA
Supply current (I_{CC_CLKS})	14 HSDS 8mA clocks enabled PLL1 and PLL2 locked.		480		mA

CLKin0/0*, CLKin1/1*和CLKin2/2*INPUT CLOCK SPECIFICATIONS

Clock input frequency (f_{CLKin})			12		MHz
Clock input slew rate ($SLEW_{CLKin}$)	20% to 80%		0.5		V/ns
Clock input Differential input voltage ($V_{IDCLKin}$)	AC coupled	0.125	1	1.55	V
Clock input Differential input voltage ($V_{SSCLKin}$)		0.25	2	3.1	V_{PP}
Clock input Single-ended input voltage (V_{CLKin})	AC coupled to CLKinX; CLKinX AC coupled to ground		1		V_{PP}
High input voltage ($V_{CLKin} - V_{IH}$)	DC coupled to CLKinX; CLKinX* AC coupled to ground		2		V
Low input voltage ($V_{CLKin} - V_{IL}$)			1		V

FBCLKin/FBCLKin* 和 Fin/Fin* INPUT SPECIFICATIONS

Clock input frequency for zero-delay with external feedback. ($f_{FBCLKin}$)	AC coupled CLKinX_TYPE=0(bipolar)		12		MHz
Clock input frequency for external VCO or distribution mode (f_{FIN})	Internal high-speed differential receiver		2600		MHz
Single ended Clock input voltage ($V_{FBCLKin/Fin}$)	AC coupled CLKinX_TYPE=0(bipolar)		1		V_{PP}
Slew rate on CLKin ($SLEW_{FBCLKin/Fin}$)	AC coupled;20% to 80% CLKinX_TYPE=0		0.5		V/ns

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
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PLL1 REFERENCE INPUT (OSC_{in}) SPECIFICATIONS

PLL1 phase detector frequency (f _{PD1})				40	MHz
PLL1 charge Pump source current (I _{CPout1} SOURCE)	V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 0		50		μA
	V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 1		150		
	V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 2		250		
					
	V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 14		1450		
	V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 15		1550		
PLL1 charge Pump sink current (I _{CPout1} SINK)	V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 0		-50		μA
	V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 1		-150		
	V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 2		-250		
					
	V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 14		-1450		
	V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 15		-1550		
Charge pump Sink / source mismatch (I _{CPout1} %MIS)	V _{CPout1} = V _{CC} /2, T = 25 °C		10%		
Magnitude of charge pump current variation vs. charge pump voltage (I _{CPout1} V _{TUNE})	0.5 V < V _{CPout1} < V _{CC} - 0.5 V, TA = 25 °C		5%		
Charge pump current vs. temperature variation (I _{CPout1} TRI)	0.5 V < V _{CPout1} < V _{CC} - 0.5 V			5	nA

PLL2 REFERENCE INPUT (OSC_{in}) SPECIFICATIONS

PLL2 reference input (f _{OSCin})			100		MHz
PLL2 reference clock minimum slew rate on OSC _{in} (SLEW _{OSCin})			0.5		V/ns
Input voltage for OSC _{in} (V _{OSCin})	AC coupled; single-ended (unused pin AC coupled to GND)		1		V _{pp}
Differential voltage swing (V _{IDOSCin})	AC coupled		1		V
Differential voltage swing (V _{SSOSCin})			2		V _{pp}
DC offset voltage (V _{OSCin} -offset)	AC coupled; Voltage difference between P-terminal and N- terminal		5		mV

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Doubler input frequency ($f_{\text{doubler_max}}$)	EN_PLL2_REF_2X OSCin duty cycle 40% = 1to (8);60%		120		MHz

CRYSTAL OSCILLATOR MODE SPECIFICATIONS

PLL2 charge pump source current ($I_{\text{CPoutSOURCE}}$)	$V_{\text{CPout2}}=V_{\text{CC}}/2$, PLL2_CP_GAIN = 0		100		μA
	$V_{\text{CPout2}}=V_{\text{CC}}/2$, PLL2_CP_GAIN = 1		400		
	$V_{\text{CPout2}}=V_{\text{CC}}/2$, PLL2_CP_GAIN = 2		1600		
	$V_{\text{CPout2}}=V_{\text{CC}}/2$, PLL2_CP_GAIN = 3		3200		
PLL2 charge pump sink current ($I_{\text{CPoutSINK}}$)	$V_{\text{CPout2}}=V_{\text{CC}}/2$, PLL2_CP_GAIN = 0		-100		μA
	$V_{\text{CPout2}}=V_{\text{CC}}/2$, PLL2_CP_GAIN = 1		-400		
	$V_{\text{CPout2}}=V_{\text{CC}}/2$, PLL2_CP_GAIN = 2		-1600		
	$V_{\text{CPout2}}=V_{\text{CC}}/2$, PLL2_CP_GAIN = 3		-3200		
Charge pump sink/source mismatch ($I_{\text{CPout2}}\% \text{MIS}$)	$V_{\text{CPout2}}=V_{\text{CC}}/2$, $T_A = 25^\circ\text{C}$		2%		
Magnitude of charge pump current vs. charge pump voltage variation ($I_{\text{CPout2}}\text{V}_{\text{TUNE}}$)	$0.5\text{ V} < V_{\text{CPout2}} < V_{\text{CC}} - 0.5\text{ V}$ $T_A = 25^\circ\text{C}$		5%		
Charge pump leakage ($I_{\text{CPout2TRI}}$)	$0.5\text{ V} < V_{\text{CPout2}} < V_{\text{CC}} - 0.5\text{ V}$		1		nA

INTERNAL VCO SPECIFICATIONS

VCO tuning range (f_{VCO})	VCO0	2370		2630	MHz/V
	VCO1	2920		3200	
VCO tuning sensitivity (K_{VCO})	VCO0 at 2457.6 MHz		30		MHz/V
	VCO1 at 2949.12 MHz		30		
Allowable temperature drift for continuous lock ($ \Delta T_{\text{CL}} $)				125	$^\circ\text{C}$

Default Power-on Reset Clock Output Frequency

Default Power-on Clock Output Frequency ($f_{\text{CLKout-startup}}$)	Default 4 6 8 10 channel open		315		MHz
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SPI Interface Timing

Table 3 SPI Interface Timing

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Setup time for SDI edge to SCLK rising edge (t_{ds})	See Figure 2	10			ns

Hold time for SDI edge from SCLK rising edge (t_{dH})	See Figure 2	10			ns
Period of SCLK (t_{SCLK})	See Figure 2	50			ns
High width of SCLK (t_{HIGH})	See Figure 2	25			ns
Low width of SCLK (t_{LOW})	See Figure 2	25			ns
Setup time for CS* falling edge to SCLK rising edge (t_{cs})	See Figure 2	10			ns
Hold time for CS* rising edge from SCLK rising edge (t_{cH})	See Figure 2	30			ns
SCLK falling edge to valid read back data (t_{dv})	See Figure 2			20	ns

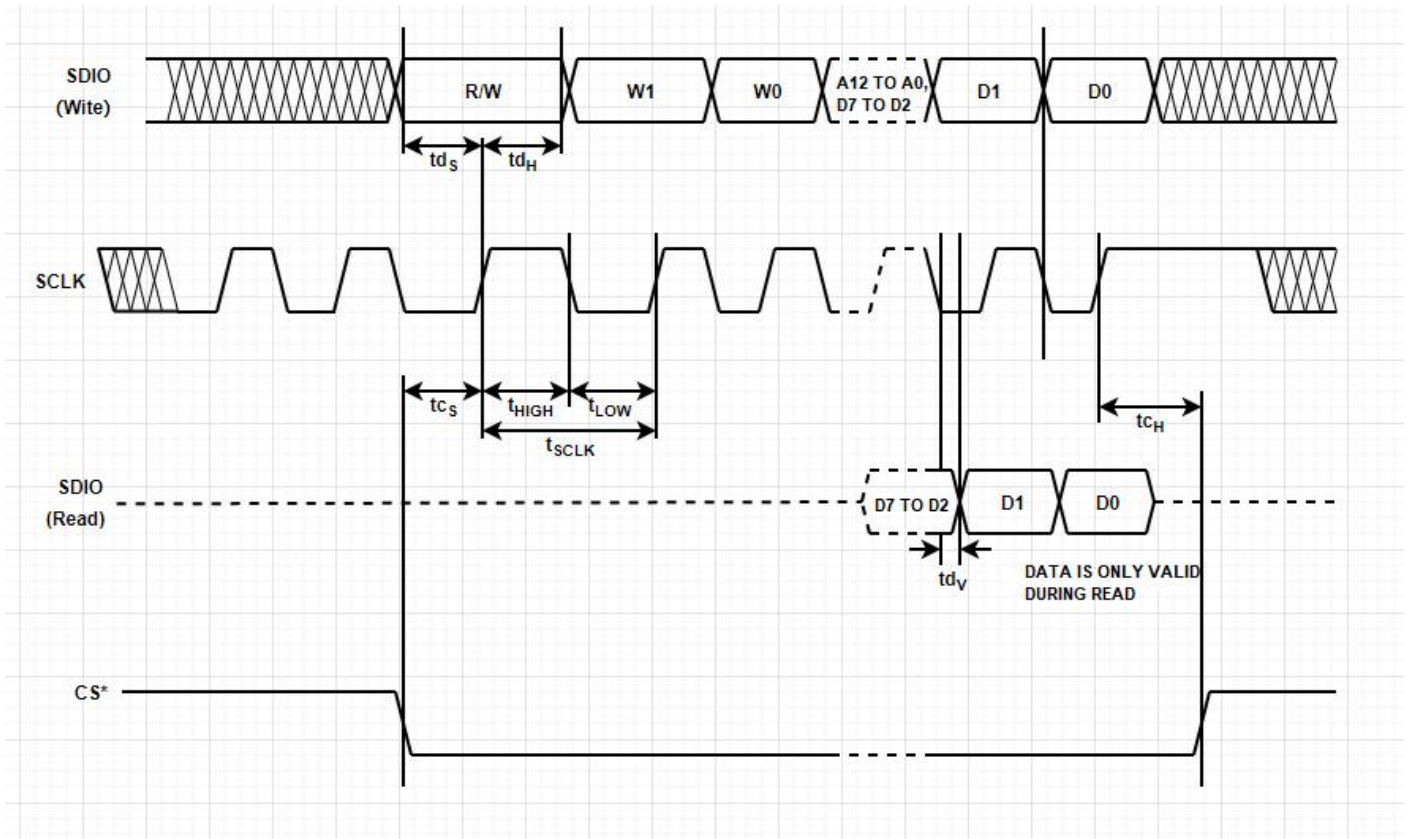
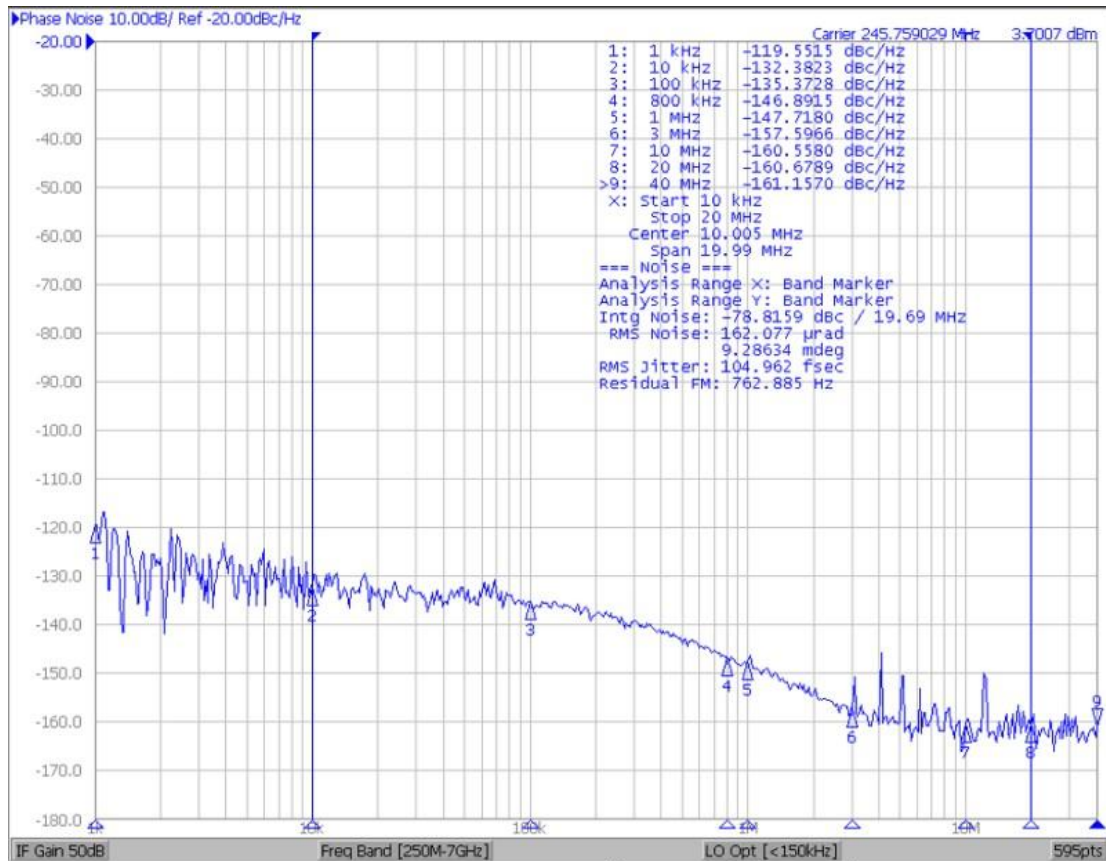


Figure 2 SPI Timing Diagram

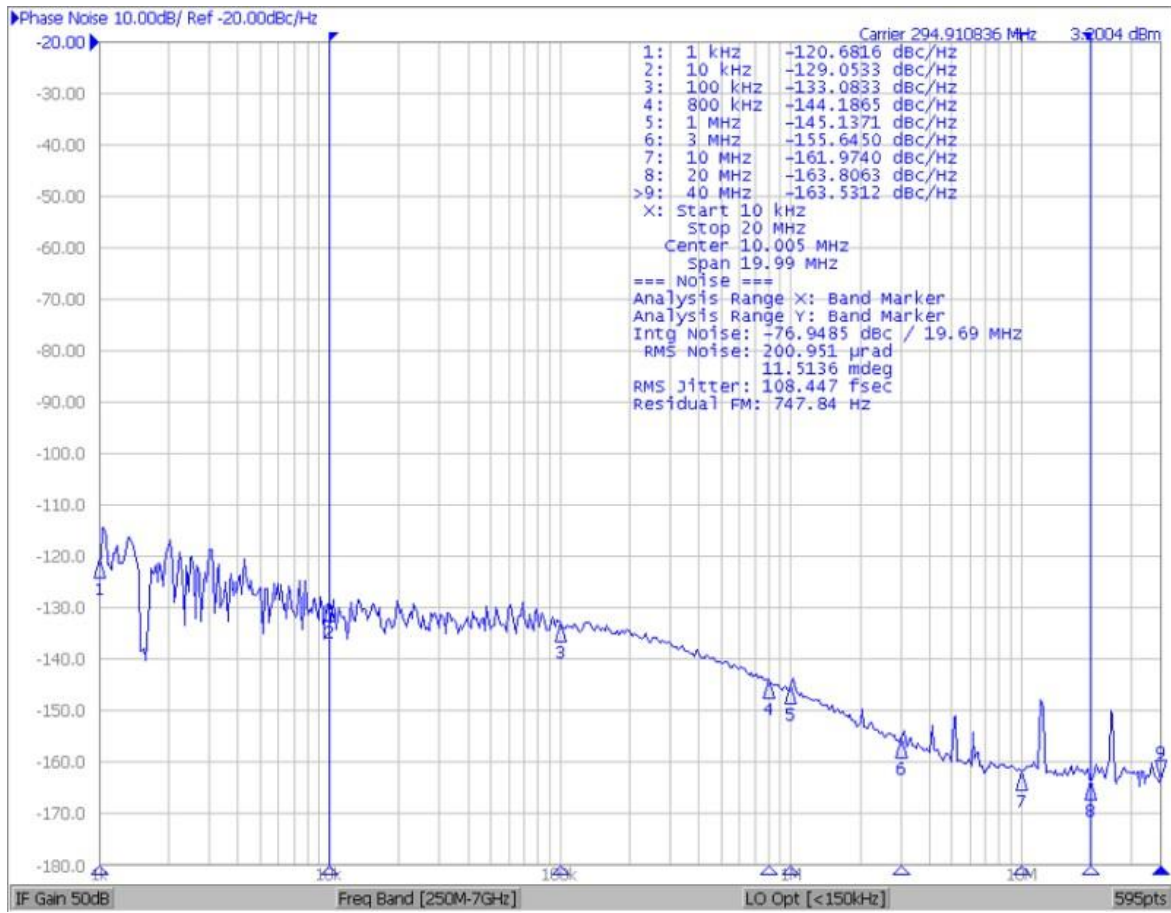
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Clock Output AC Characteristics



VCO_MUX = 0 (VCO0) PLL2 Loop Filter Bandwidth = 344 kHz
VCO0 = 2457.6 MHz PLL2 Phase Margin = 73°
DCLKout2_DIV = 10

Figure 3. DCLKout12 Phase Noise



VCO_MUX = 1 (VCO1) PLL2 Loop Filter Bandwidth = 233 kHz
VCO = 2949.12 MHz PLL2 Phase Margin = 70°
DCLKout2_DIV = 10

Figure 4. DCLKout12 Phase Noise

GX04828 PROGRAMMING

GX04828 device is programmed using 24-bit registers. Each register consists of a 1-bit command field (R/W), a 2-bit multi-byte field (W1, W0), a 13-bit address field (A12 to A0), and an 8-bit data field (D7 to D0). The contents of each register is clocked in MSB first (R/W), and the LSB (D0) last. During programming, the CS* signal is held low. The serial data is clocked in on the rising edge of the SCK signal. After the LSB is clocked in, the CS* signal goes high to latch the contents into the shift register. Recommends programming registers in numeric order – for example, 0x000 to 0x1FFF – to achieve proper device operation. Each register consists of one or more fields which control the device functionality. See Electrical Characteristics and Figure 1 for timing details.

R/W bit = 0 is for SPI write. R/W bit = 1 is for SPI read.

W1 and W0 should be written as 0.

Recommended Programming Sequence

Registers are programmed in numeric order, with 0x000 being the first and 0x1FFF being the last register programmed. The recommended programming sequence from POR involves:

1. Program register 0x000 with RESET = 1.
2. Program registers in numeric order from 0x000 to 0x165. Ensure the following register is programmed as follows: – 0x145 = 127 (0x7F)
3. Program register 0x166 to 0x1FFF.
4. Set register 0x208[1] to 1, then change the default value of 0x208[0] from 0 to 1 and to 0 again.

SYSREF_CLR

When using SYSREF output, SYSREF local digital delay block should be cleared using SYSREF_CLR bit. See SYSREF_CLR for more info.

RESET Pin

If the RESET pin is not used during normal operation, recommends programming the RESET_TYPE register to an output setting, to prevent noise from spontaneously resetting the device.

Register Maps

Register Map for Device Programming



Table 4 provides the register map for device programming. Any register can be read from the same data address it is written to.

Table 4 Register Map

ADDRESS	DATA							
[11:0]	7	6	5	4	3	2	1	0
0x000	RESET	0	0	SPI_3WIRE _DIS	0	0	0	0
0x002	0	0	0	0	0	0	0	POWER DOWN
0x003	ID_DEVICE_TYPE							
0x004	ID_PROD [15:8]							
0x005	ID_PROD [7:0]							
0x006	ID_MASKREV							
0x00C	ID_VNDR [15:8]							
0x00D	ID_VNDR [7:0]							
0x100	0	0	0	DCLKout0_DIV				
0x101	DCLKout0_DDLY_CNTH				DCLKout0_DDLY_CNTL			
0x103	DCLKout0_ADLY					DCLKout0_ ADLY_MUX	DCLKout0_MUX	
0x104	0	DCLKout 0_HS	SDCLKout 1_MUX	SDCLKout1_DDLY				SDCLKou t1_HS
0x105	0	0	0	SDCLKout1_ ADLY_EN	SDCLKout1_ADLY			
0x106	DCLKout0 _DDLY_PD	DCLKout 0_HSg_PD	DCLKout0 _ADLYg_PD	DCLKout0 _ADLY_PD	CLKou t0_1 _PD	SDCLKout1_DIS_MODE		SDCLKou t1_PD
0x107	SDCLKout 1_POL	CLKout1_FMT			DCLKo ut0 _POL	CLKout0_FMT		
0x108	0	0	0	DCLKout2_DIV				
0x109	DCLKout2_DDLY_CNTH				DCLKout2_DDLY_CNTL			
0x10B	DCLKout2_ADLY					DCLKout2_ ADLY_MUX	DCLKout2_MUX	
0x10C	0	DCLKout 2_HS	SDCLKout 3_MUX	SDCLKout3_DDLY				SDCLKou t3_HS
0x10D	0	0	0	SDCLKout3 _ADLY_EN	SDCLKout3_ADLY			

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ADDRESS	DATA							
[11:0]	7	6	5	4	3	2	1	0
0x10E	DCLKout2 _DDL _Y _PD	DCLKout 2_HSg _PD	DCLKout2 _ADLYg_P D	DCLKout2 _ADLY_PD	CLKout 2_3 _PD	SDCLKout3_DIS_MODE		SDCLKout 3_PD
0x10F	SDCLKout 3_POL	CLKout3_FMT			DCLKout 2_POL	CLKout2_FMT		
0x110	0	0	0	DCLKout4_DIV				
0x111	DCLKout4_DDLY_CNTH				DCLKout4_DDLY_CNTL			
0x113	DCLKout4_ADLY					DCLKout4 ADLY_MUX	DCLKout4_MUX	
0x114	0	DCLKout 4_HS	SDCLKout 5_MUX	SDCLKout5_DDLY				SDCLKout 5_HS
0x115	0	0	0	SDCLKout5 _ADLY_EN	SDCLKout5_ADLY			
0x116	DCLKout4 _DDL _Y _PD	DCLKout 4_HSg_P D	DCLKout4 _ADLYg_P D	DCLKout4 _ADLY_PD	CLKout 4_5 _PD	SDCLKout5_DIS_MODE		SDCLKout 5_PD
0x117	SDCLKout 5_POL	CLKout5_FMT			DCLKout 4_POL	CLKout4_FMT		
0x118	0	0	0	DCLKout6_DIV				
0x119	DCLKout6_DDLY_CNTH				DCLKout6_DDLY_CNTL			
0x11B	DCLKout6_ADLY					DCLKout6 ADLY_MUX	DCLKout6_MUX	
0x11C	0	DCLKout 6_HS	SDCLKout 7_MUX	SDCLKout7_DDLY				SDCLKout 7_HS
0x11D	0	0	0	SDCLKout7 _ADLY_EN	SDCLKout7_ADLY			
0x11E	DCLKout6 _DDL _Y _PD	DCLKout 6_HSg_P D	DCLKout6 _ADLYg_P D	DCLKout6 _ADLY_PD	CLKout 6_7 _PD	SDCLKout7_DIS_MODE		SDCLKout 7_PD
0x11F	SDCLKout 7_POL	CLKout7_FMT			DCLKout 6_POL	CLKout6_FMT		
0x120	0	0	0	DCLKout8_DIV				
0x121	DCLKout8_DDLY_CNTH				DCLKout8_DDLY_CNTL			
0x123	DCLKout8_ADLY					DCLKout8 ADLY_MUX	DCLKout8_MUX	



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ADDRESS	DATA							
[11:0]	7	6	5	4	3	2	1	0
0x124	0	DCLKout8_HS	SDCLKout9_MUX	SDCLKout9_DDLY				SDCLKout9_HS
0x125	0	0	0	SDCLKout9_ADLY_EN	SDCLKout9_ADLY			
0x126	DCLKout8_DDLY_PD	DCLKout8_HSG_PD	DCLKout8_ADLYg_PD	DCLKout8_ADLY_PD	CLKout8_9_PD	SDCLKout9_DIS_MODE		SDCLKout9_PD
0x127	SDCLKout9_POL	CLKout9_FMT			DCLKout8_POL	CLKout8_FMT		
0x128	0	0	0	DCLKout10_DIV				
0x129	DCLKout10_DDLY_CNTH				DCLKout10_DDLY_CNTL			
0x12B	DCLKout10_ADLY					DCLKout10_ADLY_MUX	DCLKout10_MUX	
0x12C	0	DCLKout10_HS	SDCLKout11_MUX	SDCLKout11_DDLY				SDCLKout11_HS
0x12D	0	0	0	SDCKLout11_ADLY_EN	SDCLKout11_ADLY			
0x12E	DCLKout10_DDLY_PD	DCLKout10_HSG_PD	DLCLKout10_ADLYg_PD	DCLKout10_ADLY_PD	CLKout10_11_PD	SDCLKout11_DIS_MODE		SDCLKout11_PD
0x12F	SDCLKout11_POL	CLKout11_FMT			DCLKout10_POL	CLKout10_FMT		
0x130	0	0	0	DCLKout12_DIV				
0x131	DCLKout12_DDLY_CNTH				DCLKout12_DDLY_CNTL			
0x133	DCLKout12_ADLY					DCLKout12_ADLY_MUX	DCLKout12_MUX	
0x134	0	DCLKout12_HS	SDCLKout13_MUX	SDCLKout13_DDLY				SDCLKout13_HS
0x135	0	0	0	SDCLKout13_ADLY_EN	SDCLKout13_ADLY			
0x136	DCLKout12_DDLY_PD	DCLKout12_HSG_PD	DCLKout12_ADLYg_PD	DCLKout12_ADLY_PD	CLKout12_13_PD	SDCLKout13_DIS_MODE		SDCLKout13_PD
0x137	SDCLKout13_POL	CLKout13_FMT			DCLKout12_POL	CLKout12_FMT		
0x138	0	VCO_MUX		OSCout_MUX	OSCout_FMT			

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ADDRESS	DATA							
[11:0]	7	6	5	4	3	2	1	0
0x139	0	0	0	0	0	SYSREF_CLKin0_MUX	SYSREF_MUX	
0x13A	0	0	0	SYSREF_DIV [12:8]				
0x13B	SYSREF_DIV [7:0]							
0x13C	0	0	0	SYSREF_DDLY [12:8]				
0x13D	SYSREF_DDLY [7:0]							
0x13E	0	0	0	0	0	0	SYSREF_PULSE_CNT	
0x13F	0	0	0	PLL2_NCLK_MUX	PLL1_NCLK_MUX	FB_MUX		FB_MUX_EN
0x140	PLL1_PD	VCO_LD_O_PD	VCO_PD	OSCin_PD	SYSREF_GBL_PD	SYSREF_PD	SYSREF_DDLY_PD	SYSREF_PLSR_PD
0x141	DDLYd_SYSREF_EN	DDLYd12_EN	DDLYd10_EN	DDLYd7_EN	DDLYd6_EN	DDLYd4_EN	DDLYd2_EN	DDLYd0_EN
0x142	0	0	0	DDLYd_STEP_CNT				
0x143	SYSREF_DDLY_CLR	SYNC_1SHOT_EN	SYNC_PO_L	SYNC_EN	SYNC_PLL2_DLD	SYNC_PLL1_DLD	SYNC_MODE	
0x144	SYNC_DIS_SYSREF	SYNC_DIS12	SYNC_DIS10	SYNC_DIS8	SYNC_DIS6	SYNC_DIS4	SYNC_DIS2	SYNC_DIS0
0x145	0	1	1	1	1	1	1	1
0x146	0	0	CLKin2_EN	CLKin1_EN	CLKin0_EN	CLKin2_TYPE	CLKin1_TYPE	CLKin0_TYPE
0x147	CLKin_SEL_POL	CLKin_SEL_MODE			CLKin1_OUT_MUX		CLKin0_OUT_MUX	
0x148	0	0	CLKin_SEL0_MUX			CLKin_SEL0_TYPE		
0x149	0	SDIO_RD_BK_TYPE	CLKin_SEL1_MUX			CLKin_SEL1_TYPE		
0x14A	0	0	RESET_MUX			RESET_TYPE		

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ADDRESS	DATA							
[11:0]	7	6	5	4	3	2	1	0
0x14B	LOS_TIMEOUT		LOS_EN	TRACK_EN	HOLD OVER_ FORCE	MAN_DAC _EN	MAN_DAC [9:8]	
0x14C	MAN_DAC [7:0]							
0x14D	0	0	DAC_TRIP_LOW					
0x14E	DAC_CLK_MULT		DAC_TRIP_HIGH					
0x14F	DAC_CLK_CNTR							
0x150	0	CLKin _OVERRI DE	0	HOLDOVER _PLL1_DET	HOLD OVER _LOS _DET	HOLDOVER _VTUNE_DET	HOLDOV ER _HITLESS _SWITCH	HOLDOV ER_EN
0x151	0	0	HOLDOVER_DLD_CNT [13:8]					
0x152	HOLDOVER_DLD_CNT [7:0]							
0x153	0	0	CLKin0_R [13:8]					
0x154	CLKin0_R [7:0]							
0x155	0	0	CLKin1_R [13:8]					
0x156	CLKin1_R [7:0]							
0x157	0	0	CLKin2_R [13:8]					
0x158	CLKin2_R [7:0]							
0x159	0	0	PLL1_N [13:8]					
0x15A	PLL1_N [7:0]							
0x15B	PLL1_WND_SIZE		PLL1 _CP_TRI	PLL1 _CP_POL	PLL1_CP_GAIN			
0x15C	0	0	PLL1_DLD_CNT [13:8]					
0x15D	PLL1_DLD_CNT [7:0]							
0x15E	0	0	PLL1_R_DLY			PLL1_N_DLY		
0x15F	PLL1_LD_MUX					PLL1_LD_TYPE		
0x160	0	0	0	0	PLL2_R[11:8]			
0x161	PLL2_R [7:0]							
0x162	PLL2_P			OSCin_FREQ			PLL2_XT AL_EN	PLL2_RE F_2X_EN
0x163	0	0	0	0	0	0	PLL2_N_CAL[17:16]	
0x164	PLL2_N_CAL [15:8]							

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ADDRESS	DATA							
[11:0]	7	6	5	4	3	2	1	0
0x165	PLL2_N_CAL [7:0]							
0x166	0	0	0	0	0	PLL2_FCAL_D IS	PLL2_N[17:16]	
0x167	PLL2_N [15:8]							
0x168	PLL2_N [7:0]							
0x169	0	PLL2_WND_SIZE		PLL2_CP_GAIN		PLL2_CP_POL	PLL 2_CP_TRI	1
0x16A	0	SYSREF_ REQ_EN	PLL2_DLD_CNT [15:8]					
0x16B	PLL2_DLD_CNT [7:0]							
0x16C	0	0	PLL2_LF_R4			PLL2_LF_R3		
0x16D	PLL2_LF_C4				PLL2_LF_C3			
0x16E	PLL2_LD_MUX					PLL2_LD_TYPE		
0x171	1	0	1	0	1	0	1	0
0x172	0	0	0	0	0	0	1	0
0x173	0	PLL2_PR E_PD	PLL2_PD	0	0	0	0	0
0x174	0	0	0	VCO1_DIV				
0x17C	OPT_REG_1							
0x17D	OPT_REG_2							
0x182	0	0	0	0	0	RB_PLL1_LD_ LOST	0	0
0x183	0	0	0	0	0	RB_PLL2_LD_ LOST	0	0
0x184	RB_DAC_VALUE [9:8]		RB_CLKin 2_SEL	RB_CLKin1_ SEL	RB_CL Kin0_ SEL	X	RB_CLKi n1_LOS	RB_CLKi n0_LOS
0x185	RB_DAC_VALUE [7:0]							
0x188	0	0	0	RB_HOLD OVER	X	X	X	X
0x1FFD	SPI_LOCK [23:16]							
0x1FFE	SPI_LOCK [15:8]							
0x1FFF	SPI_LOCK [7:0]							

PIN CONFIGURATION AND FUNCTIONS

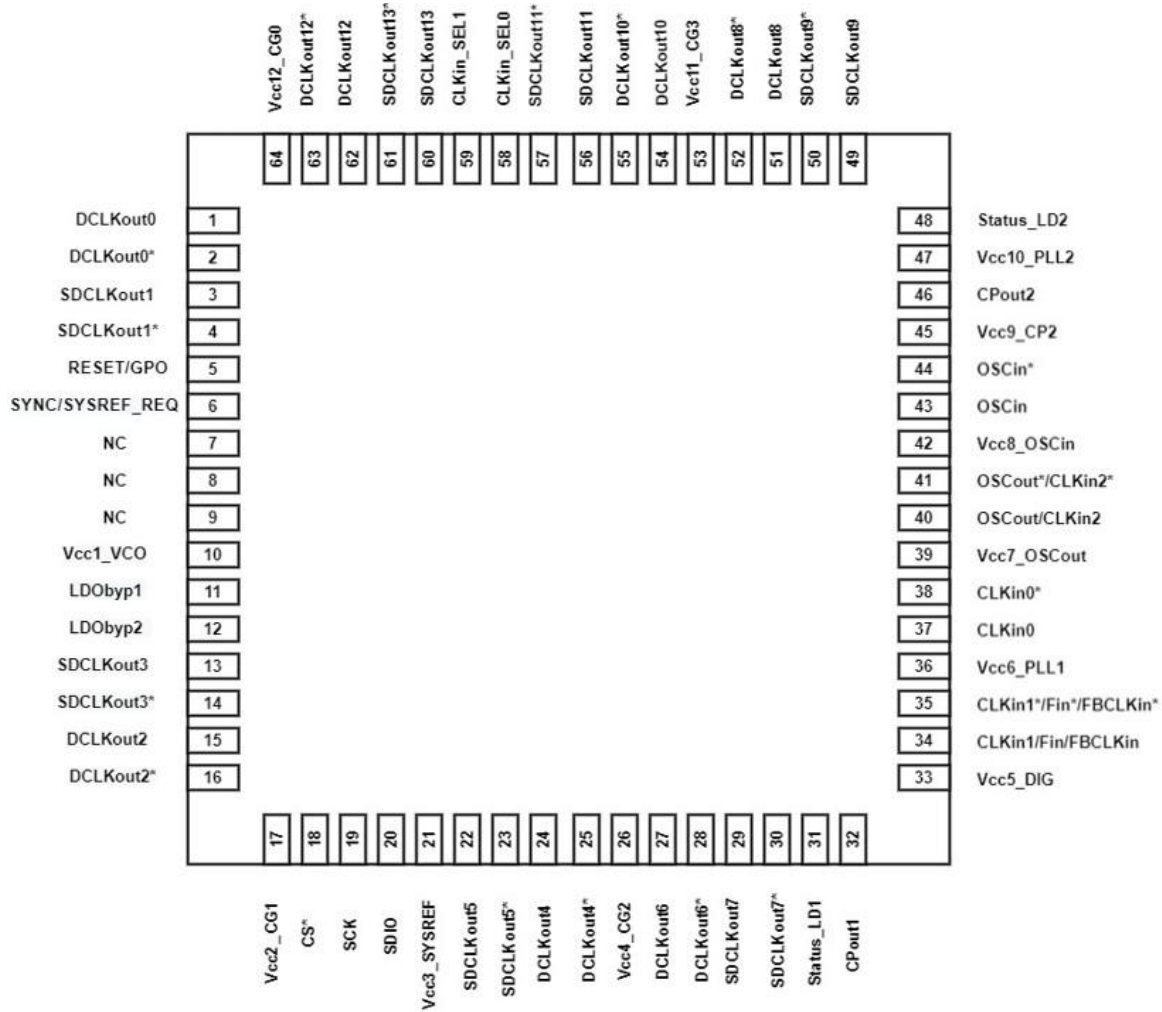


Figure 5 QFN_64 – Pin Configuration

Table 5 Pin Function Descriptions

Pin.No	Pin.Name	I/O	Description
1	DCLKout0	O	Differential clock output 0. If unused, set output format buffer to powerdown and leave pins floating.
2	DCLKout0*		
3	SDCLKout1	O	Differential clock output 1. If unused, set output format buffer to powerdown and leave pins floating.
4	SDCLKout1*		
5	RESET/GPO	I/O	Reset input or GPO. If used as a reset input, pin polarity and nominal 160-kΩ pull-up or pull-down are controlled by register settings. If used as an output, can be set to push-pull or open-drain.
6	SYNC/SYSREF_REQ	I	Synchronization input.Can be used to reset dividers, trigger the SYSREF pulser, or request continuous SYSREF from the SYSREF divider. Pin polarity is controlled by register settings. Nominal 160-kΩ pulldown.
7	-	NC	Do not connect. These pins must be left floating.
8	-	NC	
9	-	NC	

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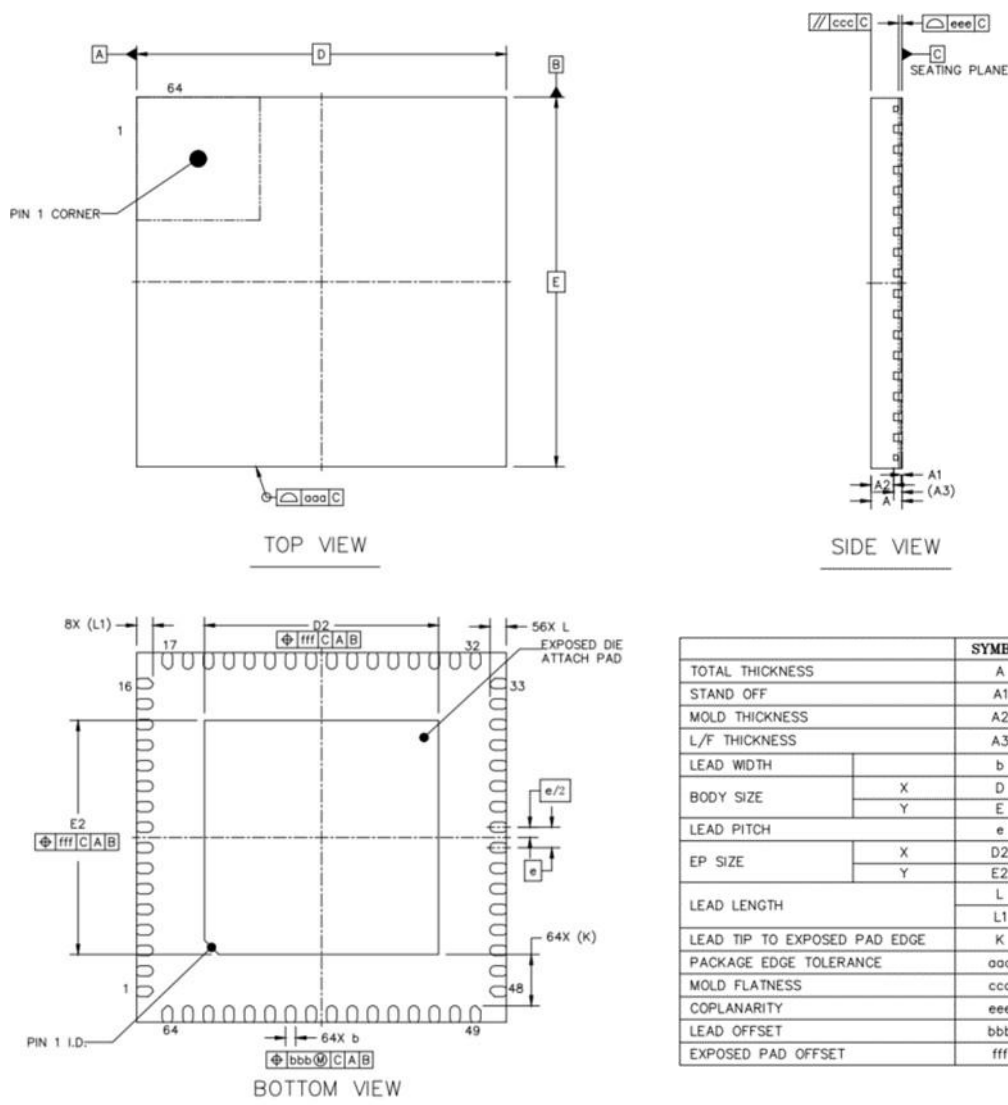
Pin.No	Pin.Name	I/O	Description
10	Vcc1_VCO	P	Power supply for VCO LDO. Decoupling capacitance requirements may change with system frequency.
11	LDObyp1	BP	LDO bypass. This pin must be bypassed to ground with 10-μF capacitor placed close to the pin.
12	LDObyp2	BP	LDO bypass. This pin must be bypassed to ground with a 0.1-μF capacitor placed close to the pin.
13	SDCLKout3	O	Differential clock output3. If unused, set output format buffer to powerdown and leave pins floating.
14	SDCLKout3*		
15	DCLKout2	O	Differential clock output2. If unused, set output format buffer to powerdown and leave pins floating.
16	DCLKout2*		
17	Vcc2_CG1	P	Power supply for clock outputs 2 and 3. Decoupling capacitance requirements may change with system frequency.
18	CS*	I	SPI Chip select. Active-low input. Must be pulled up externally or actively driven high when not in use.
19	SCK	I	SPI clock. Active-high input. Nominal 160-kΩ pulldown
20	SDIO	I/O	SPI data. This pin can be configured for open-drain or push-pull. Open-drain output requires external pull-up. Register settings can disable the output feature of this pin. Other GPIO pins can also be configured as SPI MISO (master-in slave-out) for traditional 4-wire SPI.
21	Vcc3_SYSREF	P	Power supply for SYSREF and SYNC.
22	SDCLKout5	O	Differential clock output5. If unused, set output format buffer to powerdown and leave pins floating.
23	SDCLKout5*		
24	DCLKout4	O	Differential clock output4. If unused, set output format buffer to powerdown and leave pins floating.
25	DCLKout4*		
26	Vcc4_CG2		Power supply for clock outputs 4, 5, 6, and 7.
27	DCLKout6	O	Differential clock output6. If unused, set output format buffer to powerdown and leave pins floating.
28	DCLKout6*		
29	SDCLKout7	O	Differential clock output7. If unused, set output format buffer to powerdown and leave pins floating.
30	SDCLKout7*		
31	Status_LD1	I/O	Programmable status pin. By default, this pin is configured as an active-high output representing the state of PLL1 lock detect. This pin can be configured for open-drain or push-pull output.
32	CPout1	O	Charge pump 1 output. This pin is connected to the external loop filter components for PLL1, and to the VCXO control voltage pin.
33	Vcc5_DIG	P	Power supply for digital circuitry, such as SPI bus and GPIO pins.
34	CLKin1	I	(Default) Reference clock input port 1 for PLL1. Can be configured for DC or AC coupling. Accepts single-ended or differential clocks. If unused in single-ended configuration, connect to GND with a 0.1-μF capacitor. Leave floating if both pins are unused.
	FBCLKin	I	Feedback input for external clock. Can be configured for DC or AC coupling. Accepts single-ended or differential clocks. If unused in single-ended configuration, connect to GND with a 0.1-μF capacitor. Leave floating if both pins are unused.
	Fin	I	Clock input. Can be configured for DC or AC coupling. Accepts single-ended or differential clocks. If unused in single-ended configuration, connect to GND with a 0.1-μF capacitor. Leave floating if both pins are unused.
35	CLKin1*	I	(Default) Reference clock input port 1 for PLL1. Can be configured for DC or AC coupling. Accepts single-ended or differential clocks. If

Pin.No	Pin.Name	I/O	Description
			unused in single-ended configuration, connect to GND with a 0.1-μF capacitor. Leave floating if both pins are unused.
	FBCLKin*	I	Feedback input for external clock. Can be configured for DC or AC coupling. Accepts single-ended or differential clocks. If unused in single-ended configuration, connect to GND with a 0.1-μF capacitor. Leave floating if both pins are unused.
	Fin*	I	Clock input. Can be configured for DC or AC coupling. Accepts single-ended or differential clocks. If unused in single-ended configuration, connect to GND with a 0.1-μF capacitor. Leave floating if both pins are unused.
36	Vcc6_PLL1	P	Power supply for PLL1, charge pump 1
37	CLKin0	I	Reference clock input port 0 for PLL1. Can be used as a synchronization input.
38	CLKin0*		
39	Vcc7_OSCout	P	Power supply for OSCout port and CLKin2.
40	OSCout	I/O	Output of OSCin port. Defaults to LVPECL. Only supports 240-Ω emitter resistors. If unused, set output format buffer to powerdown and leave pins floating.
	CLKin2		Reference clock input port 2 for PLL1. Can be configured for DC or AC coupling. Accepts single-ended or differential clocks. If unused in single-ended configuration, connect to GND with a 0.1-μF capacitor. Leave floating if both pins are unused. Registers must be configured to set this pin as an input.
41	OSCout*	I/O	(Default) Buffered output of OSCin port. Defaults to LVPECL. Only supports 240-Ω emitter resistors. If unused, set output format buffer to powerdown and leave pins floating.
	CLKin2*		Reference clock input port 2 for PLL1. Can be configured for DC or AC coupling. Accepts single-ended or differential clocks. If unused in single-ended configuration, connect to GND with a 0.1-μF capacitor. Leave floating if both pins are unused. Registers must be configured to set this pin as an input.
42	Vcc8_OSCin	P	Power supply for OSCin. Decoupling capacitance requirements may change with system frequency.
43	OSCin	I	Reference input to PLL2. Inputs to this pin should be AC-coupled. Accepts single-ended or differential clocks. If unused in single-ended configuration, connect to GND with a 0.1-μF capacitor. Leave floating if both pins are unused.
44	OSCin*		
45	Vcc9_CP2	P	Power supply for PLL2 charge pump.
46	CPout2	O	Charge pump 2 output. This pin is connected to the external components of the PLL2 loop filter. If an external VCO is used, this pin is also connected to the external VCO control voltage pin. Do not route this pin near noisy signals
47	Vcc10_PLL2	P	Power supply for PLL2.
48	Status_LD2	I/O	Status pin. By default, this pin is configured as an active-high output representing the state of PLL2 lock detect.
49	SDCLKout9	O	SYSREF / Device clock 9. Differential clock output.
50	SDCLKout9*		
51	DCLKout8	O	Device clock output 8. Differential clock output.
52	DCLKout8*		

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Pin.No	Pin.Name	I/O	Description
53	Vcc11_CG3	P	Power supply for clock outputs 8, 9, 10, and 11.
54	DCLKout10	O	Device clock output 10. Differential clock output.
55	DCLKout10*		
56	SDCLKout11	O	SYSREF / Device clock output 11. Differential clock output.
57	SDCLKout11*		
58	CLKin_SEL0	I/O	Programmable status pin. By default this pin is programmed as an active-high input with nominal 160-k Ω pulldown that selects which CLKin is used as the reference to PLL1 in pin-select mode. If used as an input, pin polarity and nominal 160-k Ω pull-up or pull-down are controlled by register settings. If used as an output, can be set to push-pull or opendrain
59	CLKin_SEL1	I/O	Programmable status pin. By default this pin is programmed as an active-high input with nominal 160-k Ω pulldown that selects which CLKin is used as the reference to PLL1 in pin-select mode. If used as an input, pin polarity and nominal 160-k Ω pull-up or pull-down are controlled by register settings. If used as an output, can be set to push-pull or open drain.
60	SDCLKout13	O	SYSREF / Device clock output 13. Differential clock output.
61	SDCLKout13*		
62	DCLKout12	O	SYSREF / Device clock output 12. Differential clock output.
63	DCLKout12*		
64	Vcc12_CG0	P	Power supply for clock outputs 0, 1, 12, and 13.
	E-PAD	G	Chip cooling pad, power reference.

OUTLINE DIMENSIONS



NOTES

- 1.REFER TO JEDEC MO-220;
- 2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
- 3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
- 4.FINISH: Cu/EP + Sn8~20s

Figure 6. Packaging Size of QFN-64

ORDERING GUIDE

Table 6. Order Information

Type	No.	OP temp	Package	Packing
GX048 28	GX04828GDLUM Y	-40~85°C	QFN-64	Tape & Reel

GX04828

DECLARATION

The above information is for reference only, and is intended to assist GXSC's customers in their research and development. GXSC reserves the right to change the above information without prior notice due to technological innovation.



联系我们:

联系人:JESSE

EMAIL:service_jesseli@gxschip.com

WECHAT:f40044269

FACEBOOK:GXSC

VK:@id836505054