1. Features

- Sample rate: 25MSPS
- 4-Channel Simultaneous Sampling ADC
- 74.2dB SNR
- 90dB SFDR
- Single 1.8V supply
- Low power: 200mW Total, 50mW per Channel
- Serial LVDS Output: One or Two Bits per Channel
- Selectable Input Ranges: $1V_{P-P}$ to $2V_{P-P}$
- 800MHz Full Power Bandwidth Sampling and Hold
- Sleep and nap mode
- Serial SPI port for configuration
- 52 pin (7mm x 8mm) LGA package

2. Applications

- communication
- Cellular Base Stations
- Software Defined Radio
- Portable Medical Imaging
- Multichannel Data Acquisition

Product Selection：

- GX2170：Industrial-grade temperature range of -40~85℃
- GX2170K：Wide-temperature industrial-grade temperature range of -55~125℃

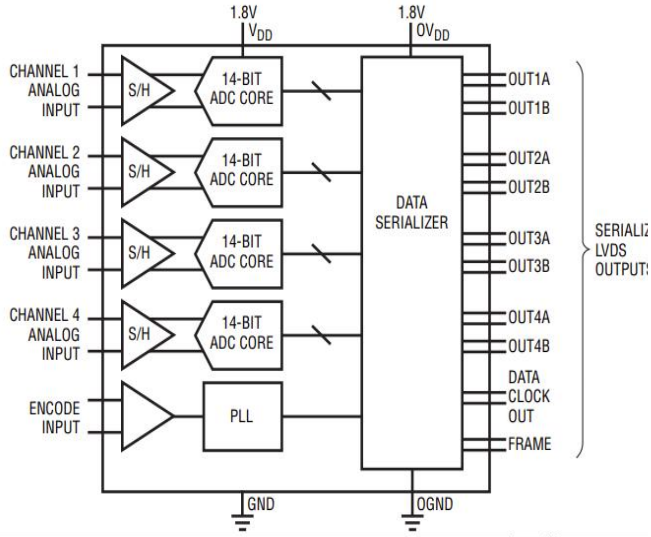


Figure 1 Functional block diagram

3. Description

The GX2170 is a 4-channel simultaneous sampling 14-bit A/D converter designed for digitizing high frequency, wide dynamic range signals.

They are perfect for demanding communications applications with AC performance that includes 74.2dB SNR and 90dB spurious free dynamic range (SFDR). DC specifications include ±1.5LSB INL(typical), ±0.4LSB DNL(typical), and it has no missing code over temperature. The transition noise is a low 1.2LSBRMS and the jitter is extremely low 0.15ps RMS.

The digital outputs are serial LVDS, with two outputs per channel at a time (2-lane mode), The LVDS driver have optional internal terminations and adjustable output levels to ensure clean signal integrity.

The ENC+ and ENC– inputs may be driven differentially or single-ended with a sine wave, PECL, LVDS, TTL or CMOS inputs. An internal clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

25Msps, dual tone FFT
f_{IN}=4.8MHz 和 5.2MHz

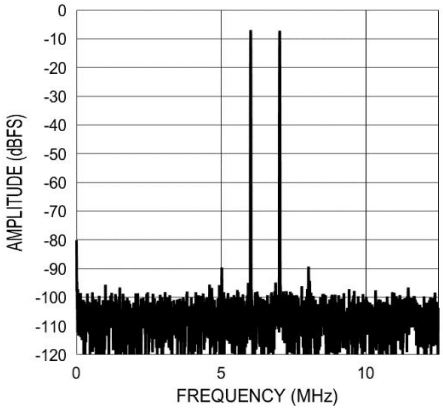


Figure 2

Catalogue

4. Absolute Maximum Ratings

Parameter	Range	Units
Supply voltage,V_{DD},OV_{DD}	−0.3 ~ 2	V
Analog input voltage AIN^+, AIN^-, PAR/$\overline{SER}$, SENSE (Note 3)	−0.3 ~ VDD+0.2	V
Digital input voltage (ENC^+, ENC^-, CS, SDI, SCK) (Note 4)	−0.3 ~ 3.9	V
Digital Output Voltage (SDO) (Note 4)	−0.3 ~ 3.9	V
Digital Output voltage	−0.3 ~ V_{DD}+0.3	V
Operating temperature range	−40 ~ 85	℃
Storage temperature range	−65 ~ 150	℃
ESD (HBM)	2000	V

Table 1 (Notes 1, 2)

5. Converter Characteristics

Where marked ● indicates that the pointer is suitable for the entire operating temperature range, otherwise it only refers to T_A=25℃ (Note 5)

Symbol	Parameter	Condition		Min	Typ	Max	Units
	Resolution (no missing codes)		●		14		Bits
INL	Integral Linearity Error	Differential analog input (Note 6)	●		±1.5		LSB
DNL	Difference linear error	Difference analog input	●		±0.4		LSB
V_{OS}	Offset error	(Note 7)	●		3.8		mV
E_G	Gain error	Internal benchmark	●		1.8		%FS
	Offset Drift				±20		uV/℃
	Full-Scale Drift	Internal benchmark			±30		ppm/℃
		External benchmark			±10		ppm/℃
	Gain Matching	External benchmark			±0.2		%FS
	Offset Matching				±3		mV
	Transition noise	External reference			1.2		LSB_{RMS}

Table 2

6. Analog Input

Where marked ● indicates that the pointer is suitable for the entire operating temperature range, otherwise it only refers to T_A=25 ° C (Note 5).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{IN}	Analog input range (AIN^+−AIN^-)	1.7 V <V_{DD}<1.9 V	●		1 to 2		V_{P-P}
$V_{IN(CM)}$	Analog input common mode (AIN^+−AIN^-)/2	Differential analog input (Note 8)	●	0.7	1	1.27	V
V_{SENSE}	Apply SENSE external voltage reference	External reference mode	●	0.6	1.25	1.3	V
I_{INCM}	Analog input common mode current				45.05		uA
I_{IN1}	Analog input leakage current (no encode)	0 < AIN+, AIN– < VDD	●		104.4		uA
I_{IN2}	PAR/SER Input leakage current		●		34.0		uA
I_{IN3}	SENSE input leakage current	1.7V<SENSE<1.9V	●		58.8		uA
t_{AP}	Sample-and-Hold acquisition delay time	0 < PAR/SER < VDD			0		ns
t_{JITTER}	Sample-and-Hold acquisition delay jitter				0.15		PS_{RMS}
CMRR	Analog input common mode rejection ratio				51.1		dB
BW_{3dB}	Full-Power bandwidth	Figure 5 Test circuit			800		MHz

Table 3

7. Dynamic Accuracy

Where marked ● indicates that the pointer is suitable for the entire operating temperature range, otherwise it only refers to T_A=25℃ (Note 5).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
SNR	Signal-to-Noise Ratio	5MHz input	●		74.4		dBFS
		30MHz input			74.2		
		70MHz input			73.9		
		140MHz input			73.3		
SFDR	Spurious Free Dynamic Range	5MHz input	●		87.8		dBFS
		30MHz input			88.4		
		70MHz input			85.5		
		140MHz input			85.6		
S/(N+D)	Signal-to-Noise plus Distortion Ratio	5MHz input	●		74.2		dBFS
		30MHz input			74.1		
		70MHz input			72.6		
		140MHz input			72.3		

Table 4

8. Internal Reference Characteristics

Where marked ● indicates that the pointer is suitable for the entire operating temperature range, otherwise it only refers to T_A=25℃, A_{IN}=-1dBFS (Note 5).

Parameter	Test Condition	Min	Typ	Max	Units
V_{CM} Output voltage	I_{OUT} = 0		1.0		V
V_{CM} Output temperature drift			±25		ppm/℃
V_{CM} Output resistance	-600uA < I_{OUT} < 1mA		2.5		Ω
V_{REF} Output voltage	I_{OUT} = 0		1.25		V
V_{REF} Output temperature drift					ppm/℃
V_{REF} Output resistance	-400uA < I_{OUT} < 1mA		1.5		Ω
V_{REF} Line Regulation	1.7V < V_{DD} < 1.9V		0.6		mV/V

Table 5

9. Digital Input And Outputs

Where marked ● indicates that the pointer is suitable for the entire operating temperature range, otherwise it only refers to T_A=25 ° C (Note 5).

Symbol	Argument	Test Condition		Min	Typ	Max	Units
Encode Inputs (ENC^+, ENC^-)							
Differential Encode Mode (ENC– Not Tied to GND)							
V_{ID}	Differential input voltage	(Note 8)	●	0.2			V
V_{ICM}	Common mode input voltage	Internally Set	●		1.2		V
		Externally Set (Note 8)		1.1		1.6	V
V_{IN}	Input voltage range	ENC^+, ENC^- to GND	●	0.2		3.6	V
R_{IN}	Input resistance	See Figure 10			10		KΩ
C_{IN}	Input capacitance				2.4		pF
Single-Ended Encode Mode(CS, SDI, SCK in serial or parallel programming mode. SDO in parallel programming mode)							
V_{IH}	High level input voltage	V_{DD} = 1.8 V	●	1.3			V
V_{IL}	Low-level input voltage	V_{DD} = 1.8 V	●			0.6	V
I_{IN}	Input current	V_{IN}=0V to 3.6V			33		μA
C_{IN}	Input capacitance	Figure 10 Test circuit			3		pF

SDO Output (serial programming mode. Open drain output. If using SDO, you will need to use a 2kΩ pull-up resistor)							
R_{OL}	Logic low output resistance to GND	V_{DD} =1.8V, SDO=0V			200		Ω
I_{OH}	Logic high output leakage current	SDO =0V to 3.6V	●	- 10		10	μA
C_{OUT}	Output capacitance				3		pF
Digital Data Output							
V_{OD}	Differential output voltage	100Ω differential load,3mA mode	●		330		mV
		100Ω differential load,1.75mA mode	●		175		mV
V_{OS}	Common mode output voltage	100Ω differential load,3mA mode	●		1. 25		V
		100Ω differential load,1.75mA mode	●		1.25		V
R_{TERM}	On-chip termination resistance	Termination enabled, OV_{DD}=1.8V		100			Ω

Table 6

10. Power Requirements

Where marked ● indicates that the pointer is suitable for the entire operating temperature range, otherwise only (Note 9).T_A=25℃

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{DD}	Analog supply voltage	(Note 10)	●	1.7	1.8	1.9	V
OV_{DD}	Output supply voltage	(Note 10)	●	1.7	1.8	1.9	V
I_{VDD}	Analog supply current	Sine wave input	●	77.6	79.3	81.2	mA
P_{DISS}	Normal mode power	2-Lane mode, 3mA mode	●	185	200	217	mW
P_{SLEEP}	Sleep mode power			0.8	1.1	1.3	mW
P_{NAP}	Nap mode power			26.2	28.4	30.9	mW

Table 7

11. Timing Characteristics

Where marked ● indicates that the pointer is suitable for the entire operating temperature range, otherwise it only refers to T_A=25℃ (Note 5).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_s	Sampling frequency	(Note 10, note 11)	●	15		25	MHz
t_{ENCL}	ENC low time (Note 8)	Duty cycle stabilizer off	●	19	20	100	ns
		Duty cycle stabilizer on		2	20	100	
t_{ENCH}	ENC high time (Note 8)	Duty cycle stabilizer off	●	19	20	100	ns
		Duty cycle stabilizer on		2	20	100	
t_{AP}	Sample-and-hold Acquisition delay time				0		ns

Table 8 (Note 4)

Symbol	Parameter	Condition		Min	Typ	Max	Units
Digital Data Output (RTERM=100Ω differential, CL=2pF to GND [on each output])							
t_{SER}	Serial Data Bit Period	2-Lane, 14-bit serialization			1/(7•f_s)		s
t_{FRAME}	FR to DCO delay	(Note 8)	●	0.35 t_{SER}	0.5 t_{SER}	0.65 t_{SER}	s
t_{DATA}	DATA to DCO delay	(Note 8)	●	0.35 t_{SER}	0.5 t_{SER}	0.65 t_{SER}	s
t_{PD}	Propagation Delay	(Note 8)	●	0.7n+2•t_{SER}	1.1n+2•t_{SER}	1.5n+2•t_{SER}	s
t_R	Output Rise time	Data, DCO, FR, 20% to 80%			0.17		ns
t_F	Output Fall time	Data, DCO, FR, 20% to 80%			0.17		ns
	DCO cycle-to-cycle jitter	t_{SER}=1ns			60		ps_{P-P}
	Pipeline latency				8		Cycles

Table 9

Symbol	Parameter	Condition		Min	Typ	Max	Units
SPI Port Timing (Note 8)							
t_{SCK}	SCK Period	Write Mode	●	40			ns
		Readback mode, C_{SDO}=20pF, R_{PULLUP}=2k	●	250			ns
t_S	$\overline{CS}$ To SCK Set-Up time		●	5			ns
t_H	SCK to $\overline{CS}$ Set-Up time		●	5			ns
t_{DS}	SDI Set-Up time		●	5			ns
t_{DH}	SDI hold time		●	5			ns
t_{DO}	SCK Falling to SDO valid	Readback mode, C_{SDO}=20pF, R_{PULLUP}=2k	●			125	ns

Table 10

Note 1: Stresses higher than the values listed in the "Absolute maximum Rating" section have the potential to cause permanent damage to the device. Prolonged exposure under any absolute maximum rating condition has the potential to affect the reliability and service life of the device.

Note 2: All voltage values are based on GND (GND and OGND short-circuits unless otherwise stated).

Note 3: When these pin voltages are pulled below GND or above V_{DD}, they will be clamped by the internal diode. This product can handle input currents greater than 100mA below GND or above V_{DD} without locking.

Note 4: When the voltage of these pins is pulled below GND, they will be clamped by the internal diode. When the voltage of these pins is

pulled above V_{DD}, they will not be clamped by the internal diode. Below GND, this product can handle input currents greater than 100mA without locking.

Note 5: V_{DD}= OV_{DD}= 1.8V, f_{SAMPLE}= 25MHz, two-wire output mode, differential ENC^+/ENC^- =$2V_{P-P}$ sine wave, input range =$2V_{P-P}$ (with differential drive), unless otherwise noted.

Note 6: Integral nonlinearity is defined as the degree to which a code deviates from the best fitted line of a transmission function curve. The deviation is measured from the center of the quantized frequency band.

Note 7: The offset error is the offset voltage measured from -0.5 LSB when the output code wobbles between 00 0000 0000 0000 and 11 1111 1111 1111 in 2's complement output mode.

Note 8: Guaranteed by design, untested.

Note 9: V_{DD}=OV_{DD}=1.8V, f_{SAMPLE}=25MHz, two-wire output mode, ENC= single-ended 1.8V square wave, ENC^-=0V, input range =$2V_{P-P}$ (with differential drive), unless otherwise noted. The power supply current and power specifications are the total value of the entire chip (not per channel).

Note 10: Recommended operating conditions.

Note 11: The maximum sampling frequency depends on the speed class of the device and the serialization mode used. The maximum serial data rate is 1000 MBPS, so t_{SER} must be greater than or equal to 1ns.

Note 12: Near channel crosstalk refers to ch.1 to ch.2 and 3 to ch.4. Far channel crosstalk refers to ch.1 to ch.3 or 4 and ch.2 to ch.3 or 4.

12. Typical Performance Characteristics

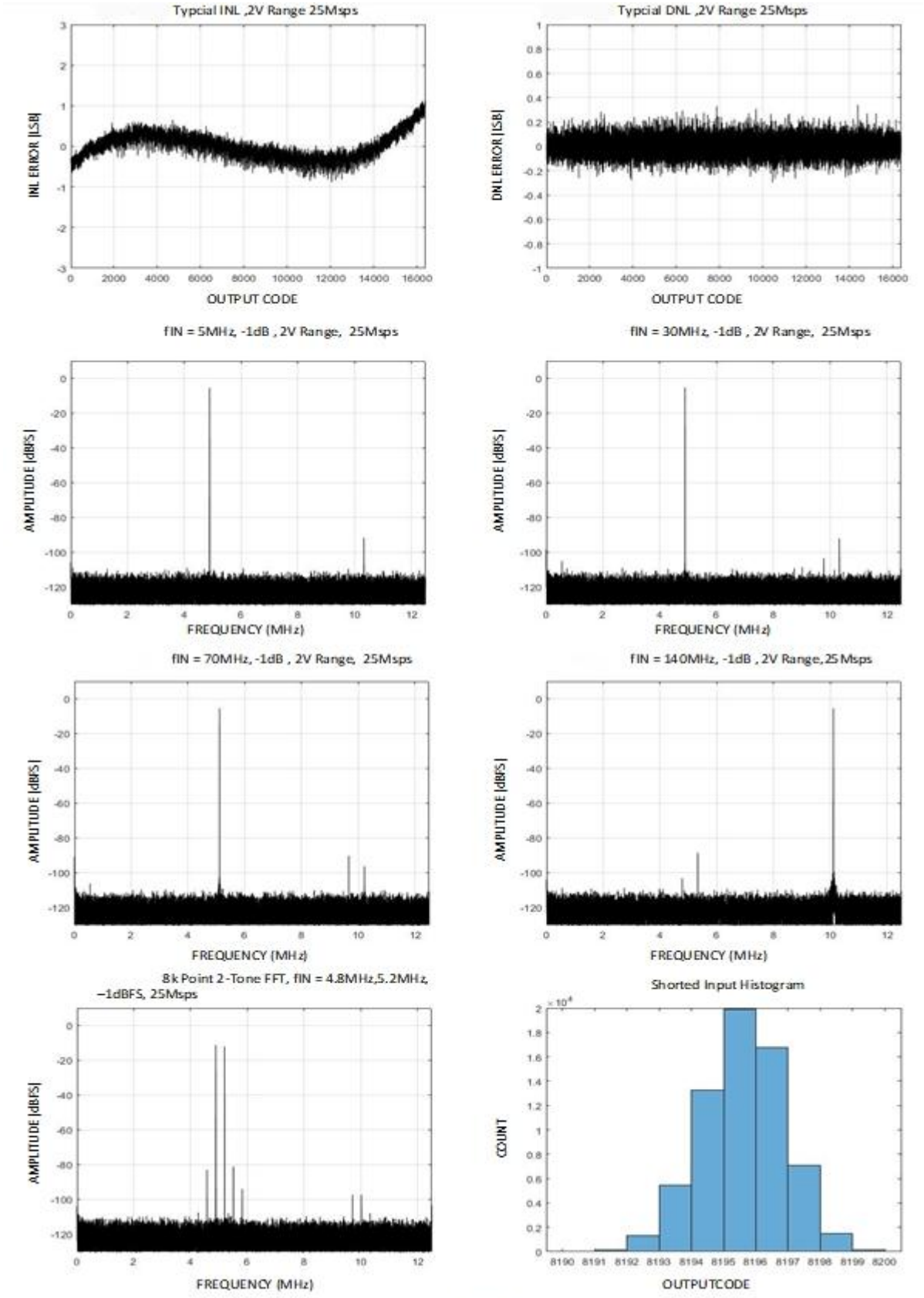


Figure 3

Figure 3

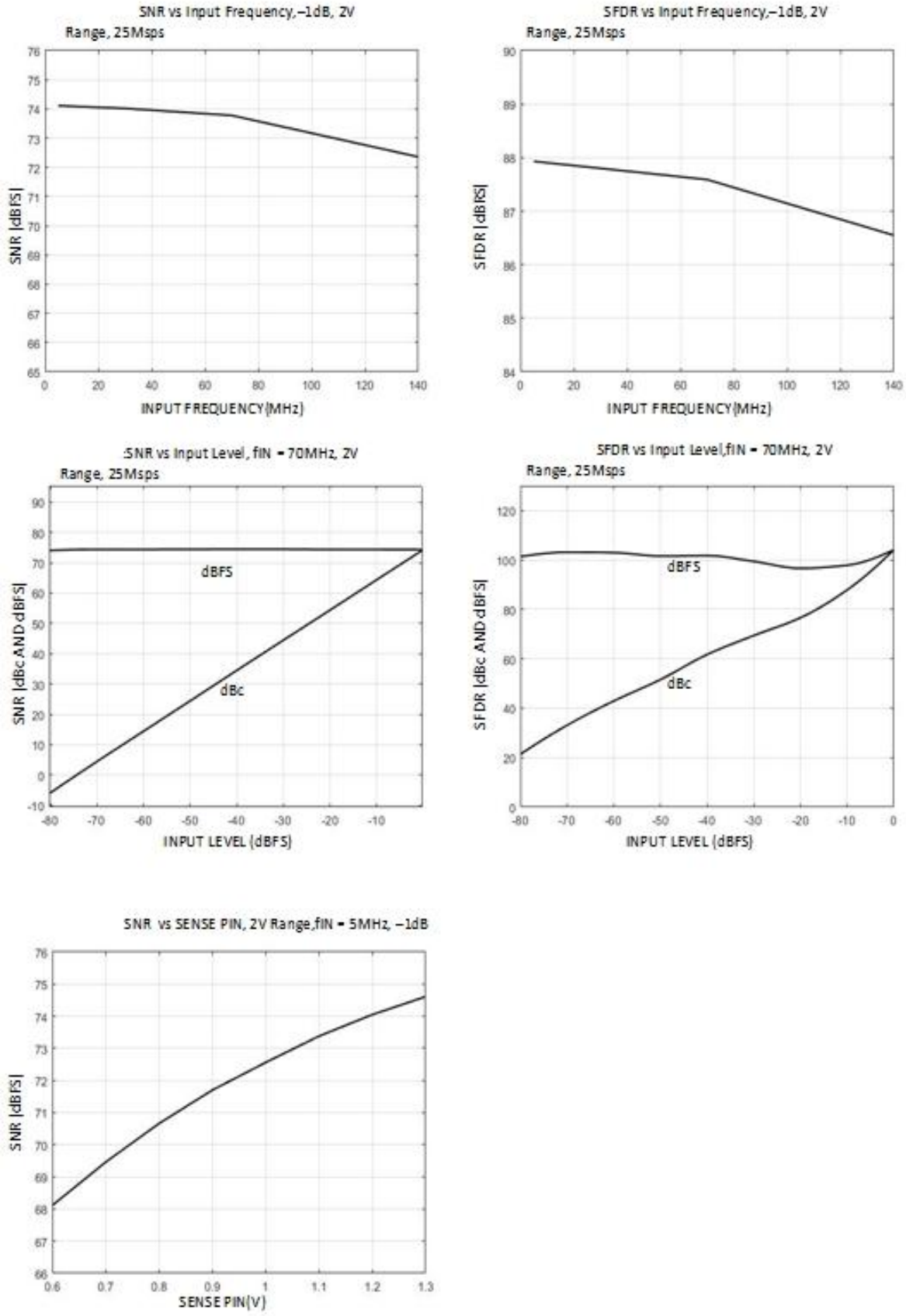

SNR vs Input Frequency,–1dB, 2V
Range, 25Msps
SNR |dBFS|
INPUT FREQUENCY(MHz)
SFDR vs Input Frequency,–1dB, 2V
Range, 25Msps
SFDR |dBFS|
INPUT FREQUENCY(MHz)
SNR vs Input Level, fIN = 70MHz, 2V
Range, 25Msps
dBFS
dBc
SNR |dBc AND dBFS|
INPUT LEVEL (dBFS)
SFDR vs Input Level,fIN = 70MHz, 2V
Range, 25Msps
dBFS
dBc
SFDR |dBc AND dBFS|
INPUT LEVEL (dBFS)
SNR vs SENSE PIN, 2V Range,fIN = 5MHz, –1dB
SNR |dBFS|
SENSE PIN(V)

Figure 4

13. Applications Information

13.1 Converter Operation

The GX2170 is a 4-channel, 14-bit, 25Msps converter powered by a single 1.8V supply. The analog input signal should be driven differentially. The encode input can be driven differentially for optimal jitter performance. The digital output are serial LVDS to minimize the number of data lines. Each channel outputs two bits at a time (2-lane mode).

13.2 Functional Block Diagram

The following diagram shows the functional block diagram of the GX2170.

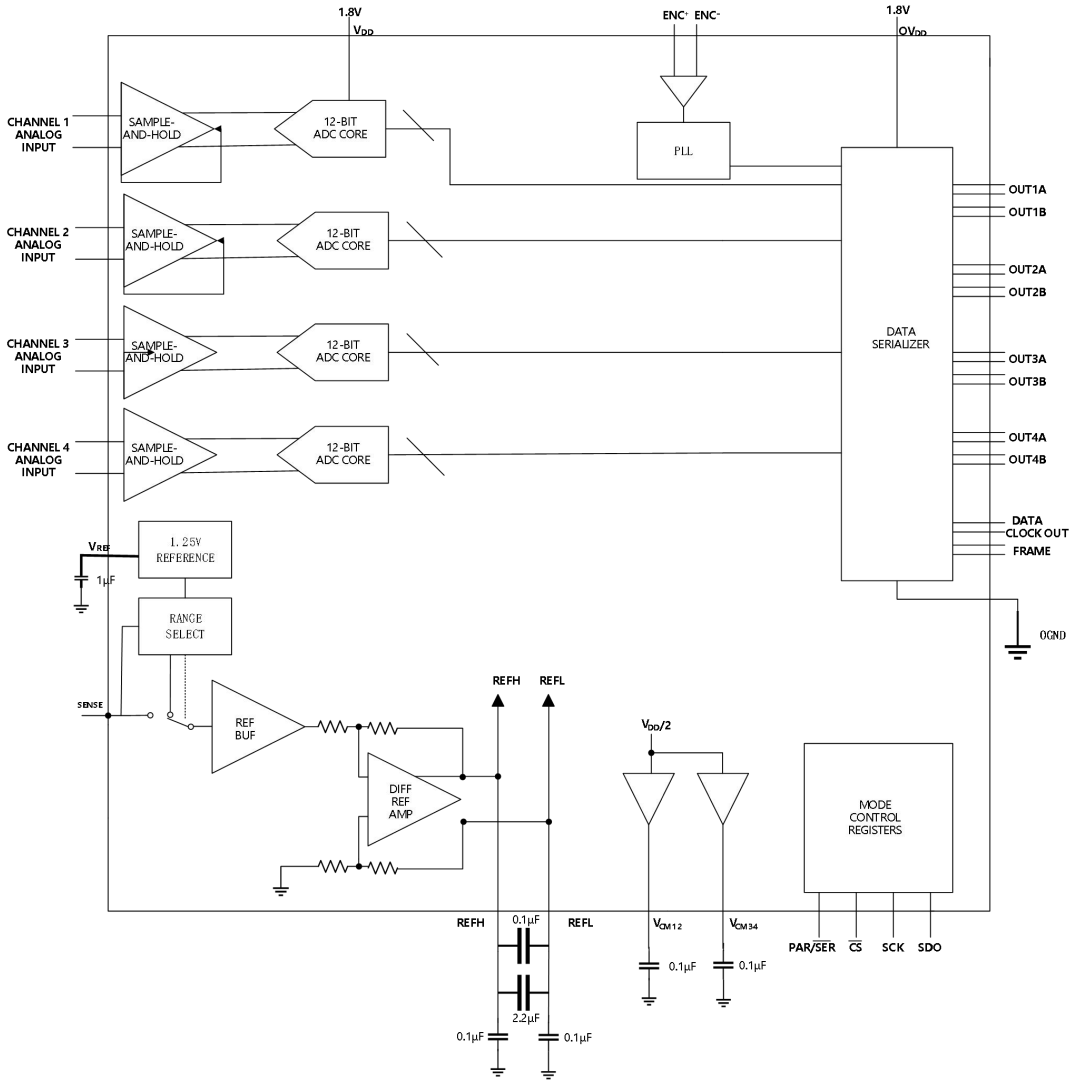


Figure 5 A 4functional block diagram of the GX2170

13.3 Timing Diagrams

The timing diagram for the GX2170 is shown below:

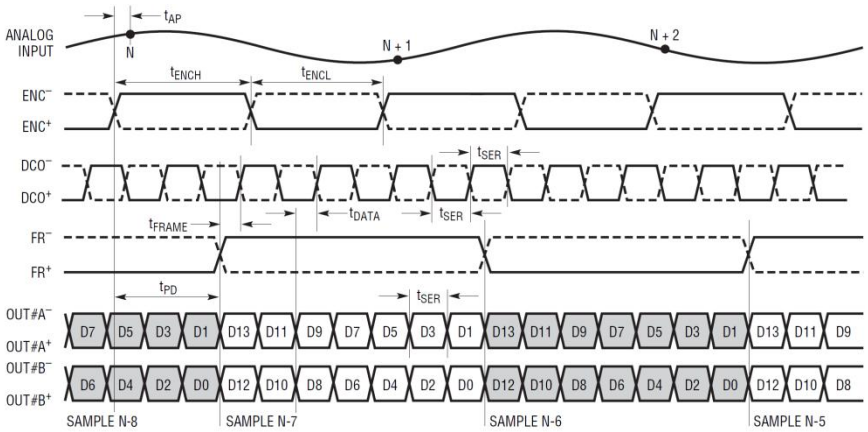


Figure 6 2-lane 14-bit serialized output mode (Note: FR^+/FR^- period is twice the ENC^+/ENC^- period in this mode)

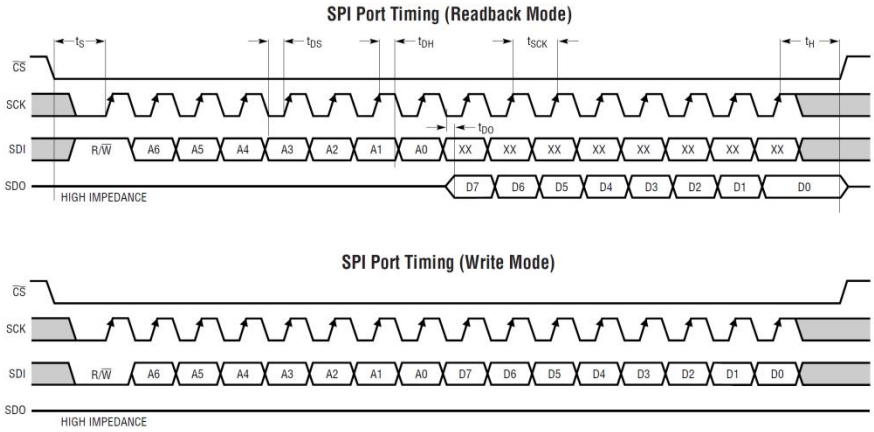


Figure 7 SPI port read/write timing

13.4 Analog Input

The analog input is a differential CMOS sample-and-hold circuits (Figure 8).The input should be driven differentially around a common mode voltage set by the V_{CM12} or V_{CM34} output pins, which are nominally $V_{DD}/2$. For the 2V input range, the input signal should swing between V_{cm}-0.5V and V_{cm}+0.5V. There should be a 180° phase difference between the inputs.

The 4 channels share a coded clock circuit for simultaneous sampling (Figure 8).

Figure 8 Equivalent input circuit. Only one of 2 analog channels is indicated

13.5 Input Drive Circuits

13.5.1 Input Filtering

If possible, there should be an RC low-pass filter right at the analog inputs. The low-pass filter isolates the drive circuit from the A/D sample-and-hold switch, and limits wideband noise from the drive circuitry. An example of the input RC filter is shown (Figure 9).

The parameter values of the RC components should be selected according to the input frequency of the applied circuit.

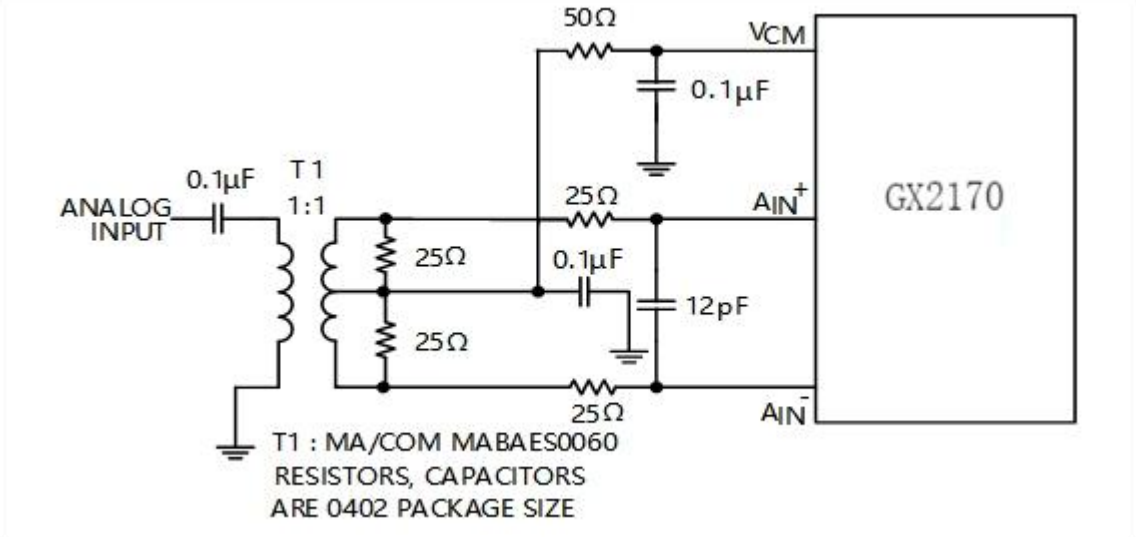


Figure 9 Analog input circuit with a transformer. Recommended for input circuits from 5MHz to 70MHz

13.5.2 Transformer Coupled Circuits

Figure 9 shows the analog input driven by an RF transformer with a center-tapped secondary. The center tap is biased with VCM, setting the A/D input at its opti mal DC level.

At higher input frequencies a transmission line balun transformers (Figures 10 to 12) have better balance, resulting in lower A/D distortion.

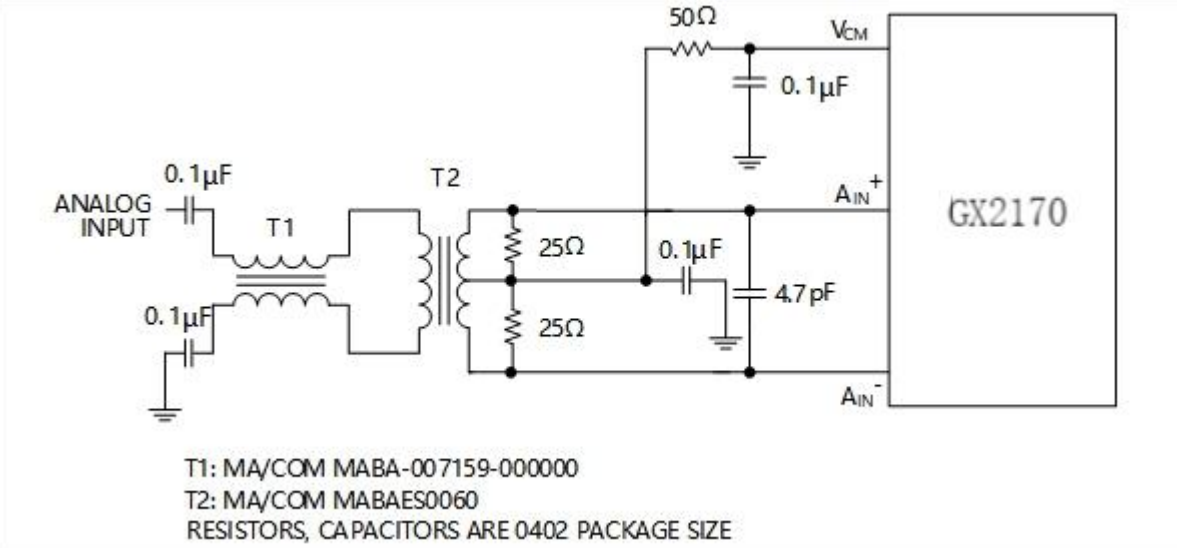


Figure 10 Recommended front-end circuits for 70MHz to 170MHz input frequencies

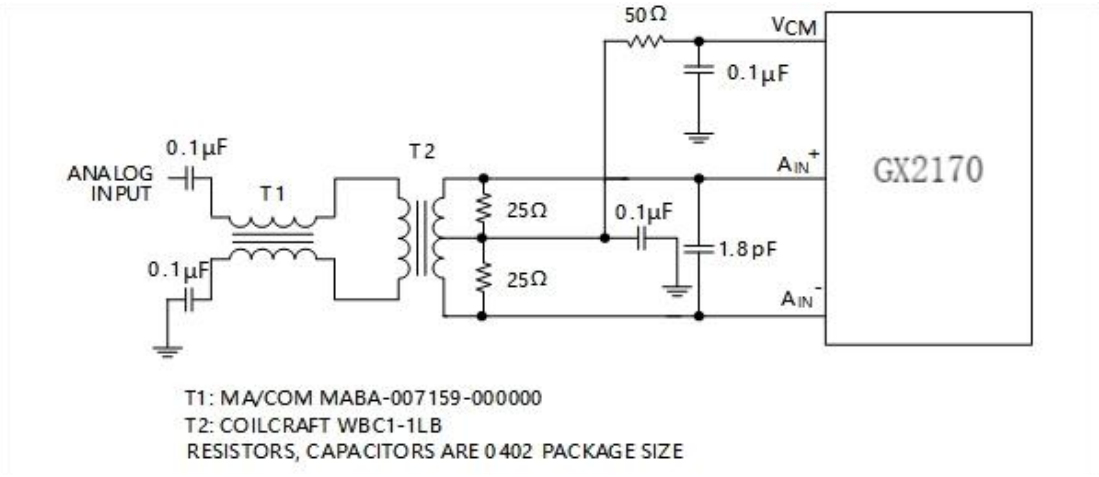


Figure 11 Recommended front-end circuits for 170MHz to 300MHz input frequencies

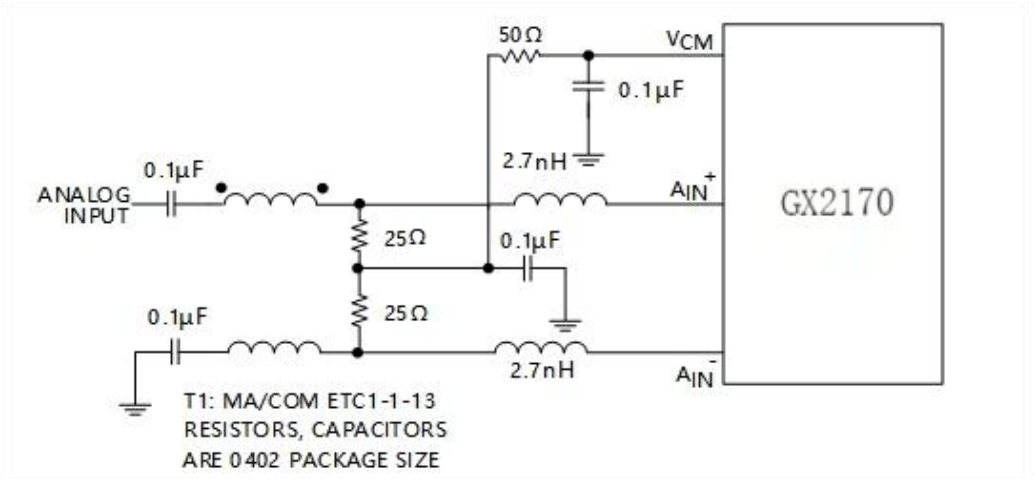


Figure 12 Recommended front-end circuits for input frequencies above 300MHz

13.5.3 Amplifier Circuits

Figure 13 shows the analog input driven by a high-speed differential amplifier. The output of the amplifier is AC-coupled to the A/D so the amplifier's output common mode voltage can be optimally set to minimize distortion.

At very high frequencies, an RF gain block will often have lower distortion than a differential amplifier. If the gain block is single-ended, then a transformer circuit (Figures 10 to 12) should convert the signal to differential before driving the A/D

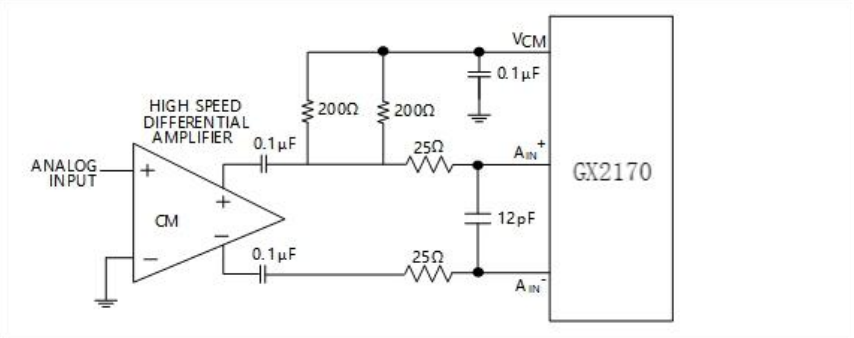


Figure 13 Uses the front end circuit of a high-speed differential amplifier

13.6 Reference

The GX2170 has an internal 1.25V voltage reference. For a 2V input range using the internal reference, connect SENSE to V_{DD}. For a 1V input range using the internal reference, connect SENSE to ground. For a 2V input range with an external reference, apply a 1.25V reference voltage to SENSE (Figure 15).

The input range can be adjusted by applying a voltage to SENSE that is between 0.625V and 1.30V. The input range will then be 1.6 • VSENSE

The reference is shared by all four ADC channels, so it is not possible to independently adjust the input range of individual channels.

The V_{REF}, REFH, and REFL pins should be bypassed, as shown in (Figure 14). The 0.1μF capacitor between the REFH and REFL should be as close to the pins as possible (not located on the back of the board).

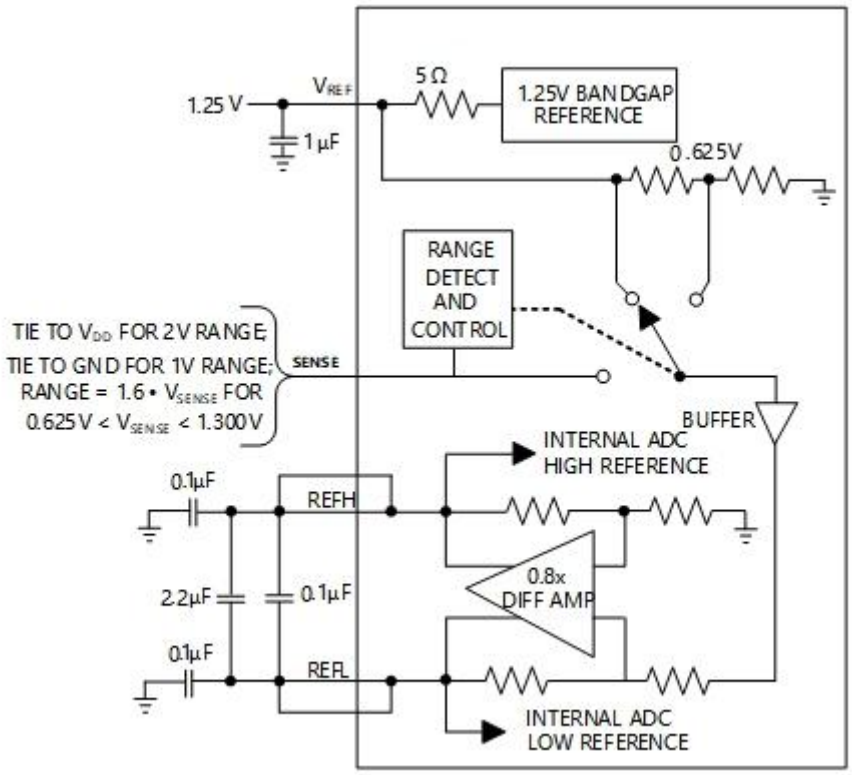


Figure 14 Reference circuit

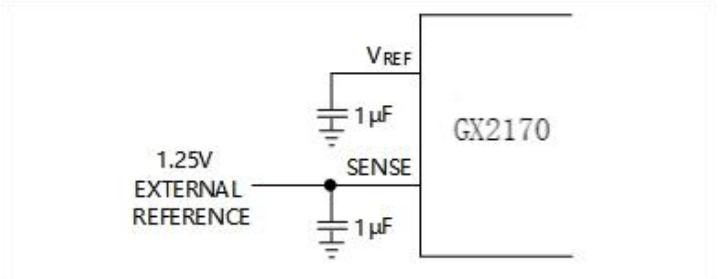


Figure 15 Uses an external 1.25V reference

13.7 Encode Input

The signal quality of the coded clock input strongly affects the A/D noise performance. The encode inputs should be treated as analog signals—do not route them next to digital traces on the circuit board The coded input is in differential coding mode (Figure 16).

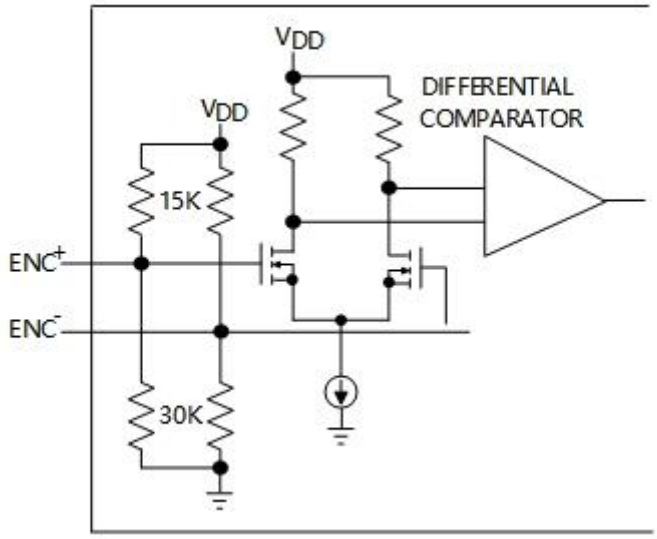


Figure 16 Equivalent coding input circuit for differential coding mode

The differential encode mode is recommended for sinusoidal, PECL, or LVDS encode inputs (Figures 17 and 18). The encode inputs are internally biased to 1.2V through 10k equivalent resistance.

The encode inputs can be taken above VDD (up to 3.6V), and the common mode range is from 1.1V to 1.6V. In the differential encode mode, ENC– should stay at least 200mV above ground to avoid falsely triggering the single-ended encode mode. For good jitter performance ENC+ should have fast rise and fall times.

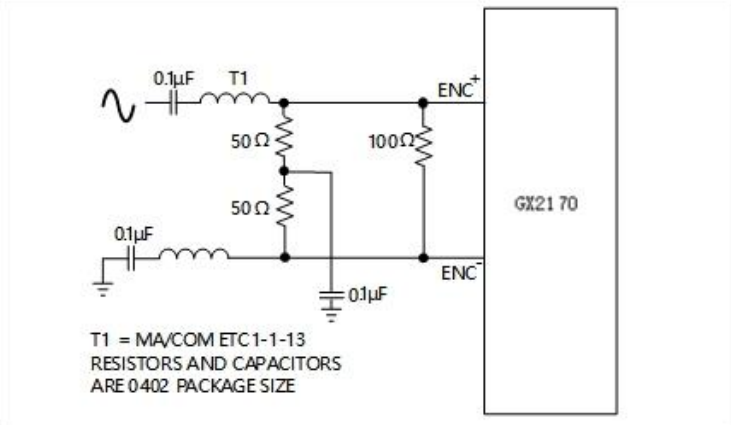


Figure 17 Sinusoidal coded drive

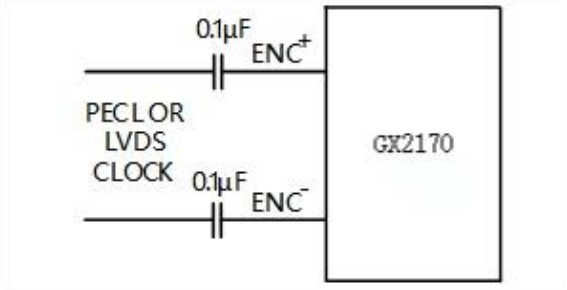


Figure 18 PECL or LVDS coded drive

13.8 Clock PLL And Duty Cycle Stabilizer

The encode clock is multiplied by an internal phase-locked loop (PLL) to generate the serial digital output data. If the encode signal changes frequency or is turned off, the PLL requires 25μs to lock onto the input clock.

A clock duty cycle stabilizer circuit allows the duty cycle of the applied encode signal to vary from 30% to 70%. In the serial programming mode it is possible to disable the duty cycle stabilizer, but this is not recommended. In the parallel programming mode the duty cycle stabilizer is always enabled.

13.9 Digital Outputs

The digital output of the GX2170 is a serialized LVDS signals. The data is processed in 16-bit or 14-bit serialization (see timing diagram for details). Each channel outputs two bits at a time via two LVDS serial ports A and B (2-lane mode). Double rate (DDR) format is used to double the output efficiency.

The DDR output data should be latched by the master processor on the rising and falling edges of the Data Clock output (DCO). The data frame output (FR) can be used to determine the starting point of the data output for each conversion result. In two-line, 14-bit serialization mode, the FR frequency is halved.

The maximum serial data rate is 1Gbps, so the maximum ADC sampling rate is limited by both the serial mode and the ADC speed class (Table 11). Table 11 6The GX2170 can achieve the highest calibrated sampling rate of 25Msps in all serial modes. The minimum sampling rate of the ADC is limited to the minimum output frequency of the internal PLL, which is 20Msps in two-wire mode.

Mode		Max Sample rate f_S (MHz)	DCO frequency	FR frequency	Serial data rate
2-wire	14-bit serialization	25	3.5, f	0.5,f_S	7,f_S

Table 11 Maximum sampling rate in serialization mode

By default, the outputs are standard LVDS levels: a 3.5mA output current and a 1.25V output common mode volt age. An external 100Ω differential termination resistor is required for each LVDS output pair. The termination resistors should be located as close as possible to the LVDS receiver.

The outputs are powered by the OV_{DD} and OGND which are isolated from the A/D core power and ground.

13.9.1 Programmable LVDS Output Current

The default output driver current is 3.5mA. This current can be adjusted by control register A2 in serial programming mode. Available current levels are 1.75mA, 2.1mA, 2.5mA, 3mA, 3.5mA, 4mA and 4.5mA. In parallel programming mode the SCK pin can select either 3.5mA or 1.75mA.

13.9.2 Optional LVDS Driver Internal Termination

In most cases, an off-chip 100Ω terminal resistor provides superior LVDS signal integrity. In addition, an internal 100Ω terminal resistor can be enabled through the mode serial programming control register A2. The internal terminal helps to absorb reflections caused by poor terminating at the receiver end. When the internal terminal is enabled, the output drive

current needs to be doubled to maintain the same output voltage swing. In parallel programming mode, the SDO pin is responsible for enabling the internal terminal. The internal terminal should only be used in 1.75mA, 2.1mA, or 2.5mA LVDS output current mode.

13.9.3 Data Format

Table 12 7shows the relationship between the analog input voltage and the digital data output bits. By default, the output data format is offset binary. The 2's complement format can be selected by serially programming mode control register A1.

(A^+_{IN}-A^-_{IN}) (2V range)	D13-D0 (Offset binary)	D13-D0 (binary complement)
> 1.000000 V	11 1111 1111 1111	01 1111 1111 1111
+ 0.999878 V	11 1111 1111 1111	01 1111 1111 1111
+ 0.999756 V	11 1111 1111 1110	01 1111 1111 1110
+ 0.000122 V	10 0000 0000 0001	00 0000 0000 0001
+ 0.000000 V	10 0000 0000 0000	00 0000 0000 0000
0.000122 V	01 1111 1111 1111	11 1111 1111 1111
0.000244 V	01 1111 1111 1110	11 1111 1111 1110
0.999878 V	00 0000 0000 0001	10 0000 0000 0001
1.000000 V	00 0000 0000 0000	10 0000 0000 0000
< 1.000000 V	00 0000 0000 0000	10 0000 0000 0000

Table 12 Relation of the output code to the input voltage

13.9.4 Digital Output Randomizer

Interference from the ADC digital output is sometimes unavoidable. It is possible for digital interference to come from capacitive or inductive coupling, or coupling through the ground plane. Even tiny coupling coefficients can cause undesired tones in the ADC output spectrum. By randomizing the digital output before it is transmitted off-chip, the amplitude of such unwanted tones can be reduced by randomizing it.

The digital output can be randomised by performing an exclusive-OR logical operation between the LSB and all other data output bits. If decoding is required, the inverse operation is applied, that is, the exclusive-OR operation is performed between the LSB and all other bits. FR and DCO outputs are not affected. The output random function generator is enabled by serial programming to the mode control register A1.

13.9.5 Digital Output Test Pattern

To allow in-circuit testing of the digital interface to the A/D, there is a test mode that forces the A/D data outputs (D13-D0) of all channels to known values. The digital output test patterns are enabled by serially programming mode control registers A3 and A4. When enabled, the test patterns override all other formatting modes: 2's complement and randomizer.

13.9.6 Output Disable

The digital outputs may be disabled by serially programming mode control register A2. The current drive for all digital outputs, including DCO and FR, are disabled to save power or enable in-circuit testing. When disabled, the common mode of each output pair becomes high impedance, but the differential impedance may remain low.

13.10 Sleep And Nap Modes

The A/D can be placed in sleep or nap mode to save power. In sleep mode the entire chip is powered off, thus achieving a power consumption of 1mW. Sleep mode is enabled by the mode control register A1 (Serial programming mode) or SDI (parallel programming mode). The length of time required to recover from sleep mode depends on the size of the bypass capacitor on the VREF, REFH, and REFL. As far as the suggested parameter values in Figure 8 are concerned, the ADC will stabilize after 2ms.

In nap mode, any combination of ADC channels can be powered off while the internal reference circuit and PLL remain operational, resulting in a faster wake up time than in sleep mode. Recovery from snooze mode requires at least

100 clock cycles. If the application requires very accurate DC stabilization, an additional 50μs time should be provided to enable the on-chip reference to stabilize from the slight temperature drift caused by the change in the supply current when the ADC is taken out of nap mode. In serial programming mode, snooze mode is enabled by mode register A1.

13.11 Device Programming Modes

The operating mode of the GX2170 can be set using a parallel interface or a simple serial interface. The serial interface provides greater flexibility and enables all available modes to be set. Parallel interfaces are more limited in that they can only set certain modes that are more commonly used.

13.11.1 Parallel Programming Mode

The use parallel programming mode, PAR/$\overline{SER}$ should be tied to V_{DD}.The $\overline{CS}$, SCK, SDI, and SDO pins are binary logic inputs that are responsible for setting certain modes of operation. These pins can be connected to V_{DD} or ground, or driven by 1.8V, 2.5V, or 3.3V CMOS logic circuits. When used as an input, the SDO should be driven by a 1k series resistor.

Pins	Description
$\overline{CS}$	**2-Lane/1-Lane Selection Bit** 0=2-Lane, 16 bit serialized output mode 1= 1-Lane, 14-bit serialized output mode
SCK	**LVDS Current selection bit** 0=3.5mA LVDS current mode 1=1.75mA LVDS current mode
SDI	**Power Down control bit** 0= Normal operation 1= Sleep mode
SDO	**Internal terminal resistance selection bit** 0= The internal termination Disabled 1= The internal termination Enabled

Table 13 Parallel Programming mode control bits (PAR/$\overline{SER}$=V_{DD})

13.11.2 Serial Programming Mode

To use the serial programming mode, PAR/SER should be tied to ground. The CS, SCK, SDI and SDO pins become a serial interface that program the A/D mode control registers. Data is written to a register with a 16-bit serial word. Data can also be read back from a register to verify its contents.

Serial data transfer starts when $\overline{CS}$ is taken low, The data on the SDI pin is latched at the first 16 rising edges of the SCK. Any SCK rising edges after the first 16 are ignored. The data transfer ends when CS is taken high again.

The first bit of the 16-bit input word is the bit. R/$\overline{W}$,The next 7 bits are the address bits of the register (A6:A0). The final 8 bits are the register data bits (D7:D0).

If the R/$\overline{W}$ bit is low, the serial data (D7:D0) will be written to the register set by the address bits (A6:A0). If the R/$\overline{W}$ bit is high, data in the register set by the address bits (A6:A0) will be read back on the SDO pin (see the Timing Diagrams section). During a readback command the register is not updated and data on SDI is ignored.

The SDO pin is an open-drain output that pulls to ground with a 200Ω impedance. If register data is read back through SDO, an external 2k pull-up resistor is required. If the serial data is only written and readback is not needed, then SDO can be left floating and no pull-up resistor is needed.

13.12 Software Reset

If serial programming is used, the mode control registers should be programmed as soon as possible after the power supplies turn on and are stable. The first serial command must be a software reset which will reset all register data bits to

logic 0. To perform a software reset, bit D7 in the reset register is written with a logic 1. After the reset SPI write command is complete, bit D7 is automatically set back to zero.

13.13 Grounding And Bypassing

The GX2170 requires a printed circuit board with a clean and complete ground plane. It is recommended to use a multilayer circuit board with an internal ground plane laid in the first circuit board under the ADC chip. The layout of the printed circuit board should ensure that the digital and analog signal lines are separated from each other as much as possible. particularly care should be taken to avoid arranging digital signal traces along the analog signal trace or underneath the ADC.

High quality ceramic bypass capacitors should be used on the V_{DD}, OV_{DD}, V_{CM}, V_{REF}, V_{DD}, REFH, and REFL pins. Bypass capacitors must be placed as close to the device pins as possible. Of particular importance are the 0.1μF capacitors laid between the REFH and the REFL. This capacitor should be located on the same side of the board as the ADC and as close to the device as possible (distance≤1.5mm).

Ceramic capacitors of 0402 specification are recommended. If a larger 2.2μF capacitor is used between the REFH and the REFL, it can be a little further away from the device. The wiring connecting the pins to the bypass capacitor must be kept short and as wide as possible.

The wiring for analog inputs, coded signals, and digital outputs must not be adjacent to each other. These signals should be isolated from each other by using ground padding and ground through-holes as barriers.

13.14 Heat Transfer

Most of the heat generated by the GX2170 is transferred from the chip to the printed circuit board through the bare bottom liner and package pins. For excellent electrical and thermal performance, the bare liner must be soldered to a large ground liner on the PCB. The liner should be connected to the internal ground plane through a series of through-holes.

14. Register Table

Register name	Address (HEX)	Data bits	Feature	Default	Initialization (HEX)
A0	00	< 7 >	**Reset** Soft reset, 1 effective	0	
		< 6:0 >	Unused, irrelevant bit	X	
A1	01	< 7 >	**DCSOFF** clock duty cycle stabilizer bit 0= Turn on clock duty cycle stabilizer 1= Turn off the clock duty cycle stabilizer	1	
		< 6 >	**RAND** data output randomized mode control bit 0= Turn off output Randomization mode 1= Turn on output randomization mode	0	
		< 5 >	**TWOSCOMP** binary complement mode control bit 0= Output binary format 1= Output 2's complement format	0	
		< 4:0 >	**SLEEP:NAP_2:1:1:NAP_1** Sleep/nap mode control bit 00000= Normal working mode (Note 1) 00001= Channel 1 in snooze mode 00010= Channel 2 in snooze mode 00100= Channel 3 in snooze mode 01000= Channel 4 in snooze mode 1XXXX= sleep mode. All channels stop working.	00110	
A2	02	< 7:5 >	**ILVDS2:ILVDS0** LVDS output current control bit 000=3.5mA LVDS Output Driver Current 001=4.0mA LVDS Output Driver Current 010=4.5mA LVDS Output Driver Current 011= unused 100=1.75 mA LVDS Output Driver Current 101=2.0 mA LVDS Output Driver Current 110=2.5 mA LVDS Output Driver Current 111=3.0 mA LVDS Output Driver Current	000	80
		< 4 >	TERMONLVDS internal terminal resistance gate 0= Do not use the on-chip LVDS terminal resistor 1= Use on-chip LVDS terminal resistors	0	
		< 3 >	**OUTOFF** outputs deactivation bits 0= normal numeric output 1= Turn off digital output	0	
		< 2 >	**OUTMODE** Digital output mode control bit 0= Two-wire 14-bit serial mode 1= Single-lane channels are not supported	0	
		<1:0>	X unused	X	
A3	03	< 7 >	**OUTTEST** Digital output test mode control bit 0= normal data output 1= Output test vector	0	
		< 6 >	X unused, irrelevant bit.	X	
		<5:0>	**TP<13:8>** Test Mode Data Bit (MSB) Used to set the highest bit 13th (MSB) to the data bit 8th of the test vector.	0	
A4	04	<7:0>	**TP<7:0>** Test Mode data bit (MSB) Used to set the highest bit 7th to data bit 0th (LSB) of the test vector.	0	
A5	05	<7:6>	Inside, not open. Hold 0000000.	0000000	
		< 1 >	Code clock receive module deactivation bit, can be used with nap mode 0= Normal operation 1= Deactivated	0	
A7	07		Inside, not open		
A8	08		Inside, not open		
A9	09		Inside, not open		
A10	0A		Inside, not open		
A11	0B		Inside, not open		

Register name	Address (HEX)	Data bits	Feature	Default	Initialization (HEX)
A12	0C		Inside, not open		
A13	0D		Inside, not open		
A14	0E		Inside, not open		
A15	0F		Inside, not open		
A16	10		Inside, not open		
A17	11		Inside, not open		

Table 14 Serial Programming mode register mapping table (" PAR/" ¯("SER")=GND)

GX2170 Recommended register configuration for 2lane: 0x00 0x80; 0x01 0x80; 0x02 0x81; 0x06 0x40 ; 0x07 0x3f ; 0x0b 0x07 ; 0x0c 0xc8.

15. Typical Application

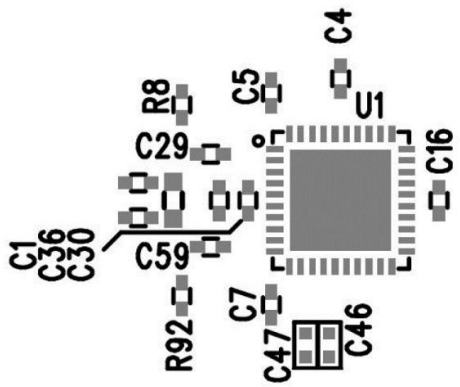


Figure 19 Top layer silk screen character diagram

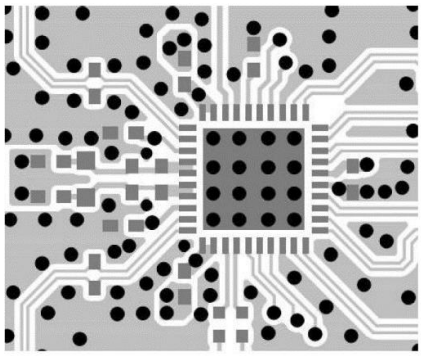


Figure 20 Top face

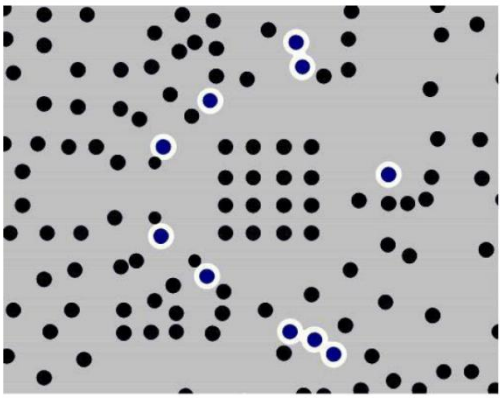


Figure 21 2nd inner layer (GND)

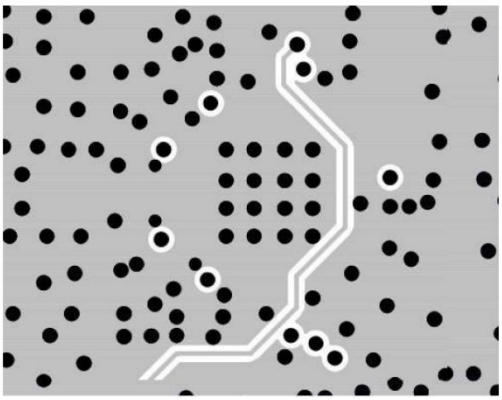


Figure 22 3rd inner layer

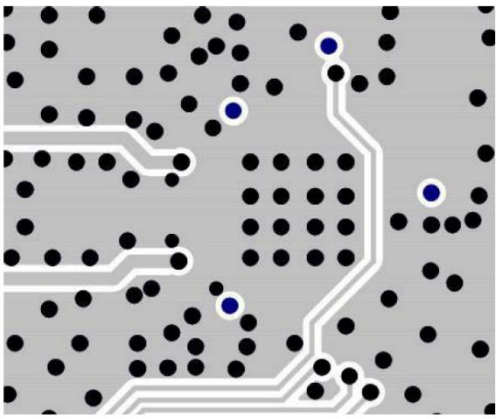


Figure 23 4th inner layer (GND)

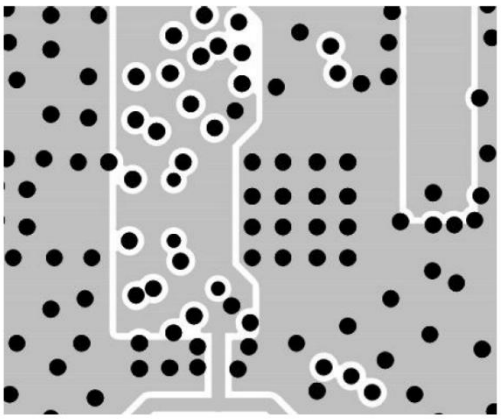


Figure 24 5th inner layer (power supply)

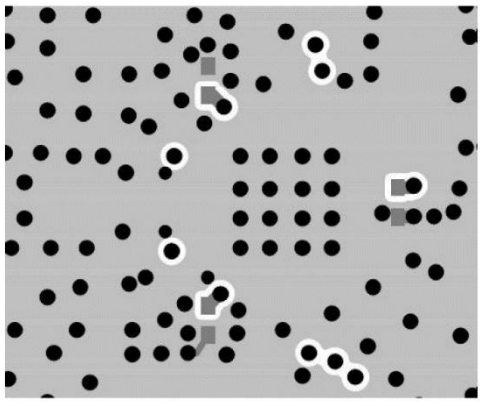


Figure 25 Bottom side

Figure 26 Bottom screen character diagram

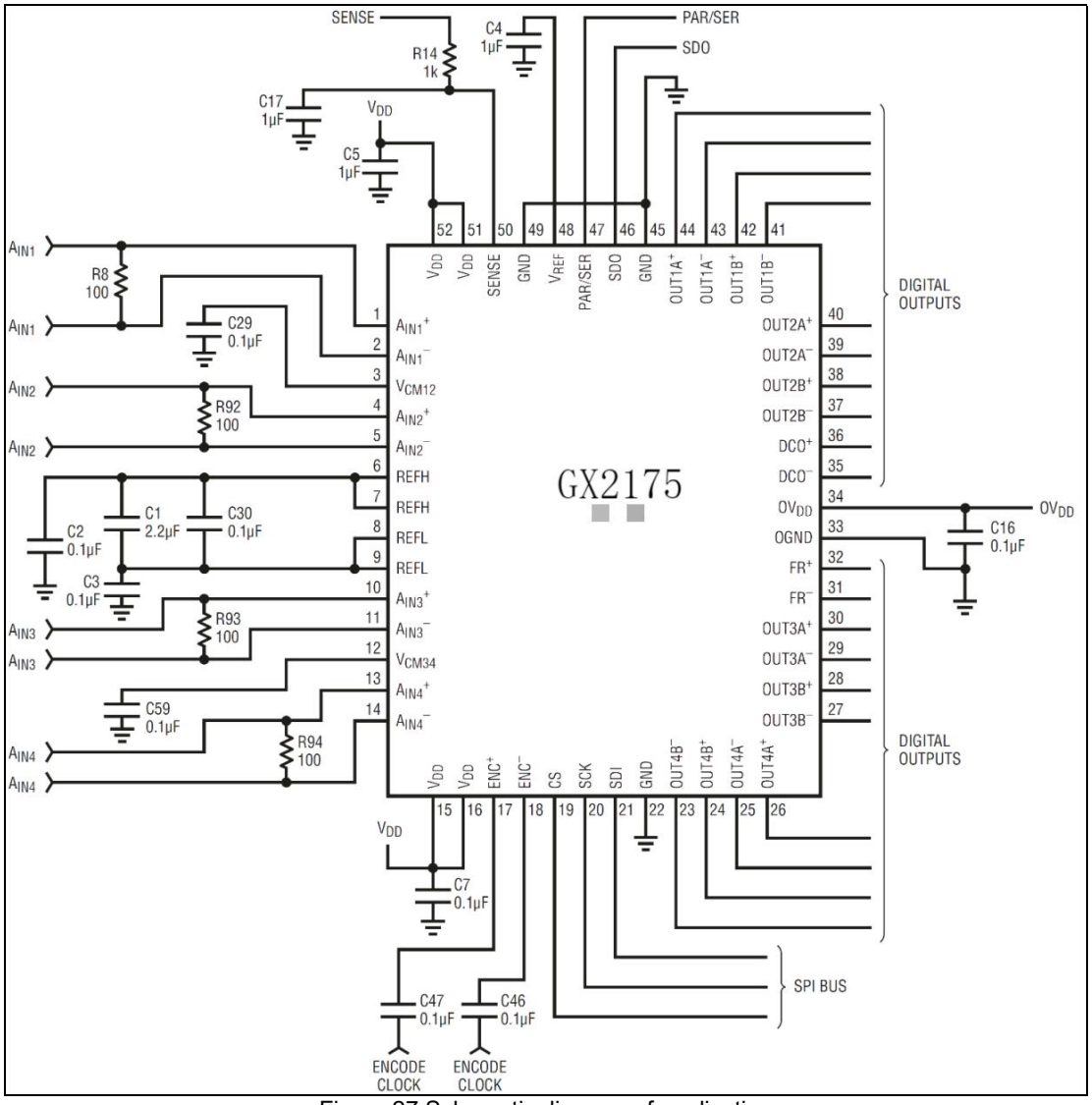
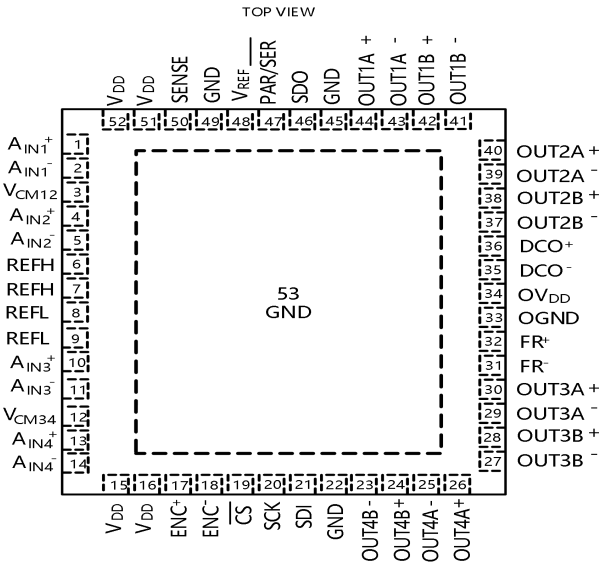


Figure 27 Schematic diagram of application

16. Pin Configuration And Function



UKG PACKAGE
52-LEAD (7mm × 8mm) PLASTIC LGA
TJMAX = 150°C, θJA = 28°C/W
EXPOSED PAD (PIN 53) IS GND, MUST BE SOLDERED TO PCB

Figure 28 LGA package 52-pin

Pin		Pin Type	Description
Name	Number		
A_{IN1+}	1	Input	Channel 1 Positive differential analog input.
A_{IN1-}	2	Input	Channel 1 Negative differential analog input.
V_{CM12}	3	Output	Common-mode biased output with a nominal value equal to $V_{DD}/2$. V_{CM} should be used to bias the common mode of analog inputs for channels 1 and 2. Bypass to ground with a 0.1μF ceramic capacitor.
A_{IN2+}	4	Input	Channel 2 Positive differential analog input.
A_{IN2-}	5	Input	Channel 2 Negative differential analog input.
REFH	Refh 6, 7	Output	ADC high level reference. Bypass to pins 8 and 9 with a 2.2μF ceramic capacitor and to ground with a 0.1μF ceramic capacitor.
REFL	Refl 8, 9	Output	ADC low level reference. Bypass to pins 6 and 7 with a 2.2μF ceramic capacitor and to ground with a 0.1μF ceramic capacitor.
A_{IN3+}	10	Input	Channel 3 Positive differential analog input.
A_{IN3-}	11	Input	Channel 3 Negative differential analog input.
V_{CM34}	12	Output	Common-mode biased output with a nominal value equal to $V_{DD}/2$. V_{CM} should be used to bias the common-mode analog inputs for channels 3 and 4. Bypass to ground with a 0.1μF ceramic capacitor.
A_{IN4+}	13	Input	Channel 4 Positive differential analog input.
A_{IN4-}	14	Input	Channel 4 Negative differential analog input.
V_{DD}	15, 16, 51, 52	Power Supply	1.8V analog power supply. Bypass the pin to ground with a 0.1μF ceramic capacitor. Adjacent pins may share a bypass capacitor.
ENC^+	17	Input	Coded clock differential positive input. The conversion operation starts at the rising edge.
ENC^-	18	Input	Code complementary input. The conversion operation starts at the falling edge.
$\overline{CS}$	19	Input	In serial programming mode, (PAR/$\overline{SER}$ =0V), $\overline{CS}$ is the serial interface chip select input. When in low power, SCK is enabled to move data on the SDI into the mode control register. In parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), $\overline{CS}$ is responsible for selecting the two-track or single-track output mode. $\overline{CS}$ can use 1.8V to 3.3V logic circuit to drive.

SCK	20	Input	In serial programming mode, (PAR/$\overline{SER}$ = 0V), SCK is the serial interface clock input. In parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SCK is responsible for selecting either 3.5mA or 1.75mA LVDS output current. SCK can be driven with 1.8V to 3.3V logic circuits.
SDI	21	Input	In serial programming mode (PAR/$\overline{SER}$ = 0V), SDI is serial interface data input. The data on SDI is timed to enter the mode control register at the rising edge of SCK. In parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SDI can be used to power off the device. SDI can be driven by 1.8V to 3.3V logic circuits.
GND	22, 45, 49, 53	Grounded	ADC power ground. Multiple through-holes should be used near these pins. The bare liner (pin 41) must be soldered to the ground of the PCB.
$OUT4B^-$	23	Output	Serial data LVDS for channel 4 outputs B-channel negative. Works in dual channel output mode.
$OUT4B^+$	24	Output	Serial data LVDS for channel 4 outputs positive B. Works in two-track output mode.
$OUT4A^-$	25	Output	Serial data LVDS for channel 4 outputs A negative terminal.
$OUT4A^+$	26	Output	Serial data LVDS for channel 4 outputs A positive terminal.
$OUT3B^-$	27	Output	Serial data LVDS for channel 3 outputs B-channel negative.Works in dual channel output mode.
$OUT3B^+$	28	Output	Serial data LVDS for channel 3 outputs positive B. Works in two-track output mode.
$OUT3A^-$	29	Output	Serial data LVDS for channel 3 outputs A negative terminal.
$OUT3A^+$	30	Output	Serial data LVDS for channel 3 outputs A positive terminal.
FR^-	31	Output	Frame differential output, negative.
FR^+	32	Output	Frame differential output, positive.
OGND	33	Grounded	Output drive ground. This pin must be shorted to the ground plane through a very low inductance path. Multiple through-holes should be used near this pin.
OV_{DD}	34	Power supply	Output drive power supply. Bypass to ground with a 0.1μF ceramic capacitor.
DCO^-	35	Output	Data clock differential output, negative.
DCO^+	36	Output	Data clock differential output, positive.
$OUT2B^-$	37	Output	Serial data LVDS for channel 2 outputs B-channel negative. Works in dual channel output mode.
$OUT2B^+$	38	Output	Serial data LVDS for channel 2 outputs positive B. Works in two-track output mode.
$OUT2A^-$	39	Output	Serial data LVDS for channel 2 outputs A negative terminal.
$OUT2A^+$	40	Output	Serial data LVDS for channel 2 outputs A positive terminal.
$OUT1B^-$	41	Output	Serial data LVDS for channel 1 outputs B-channel negative. Works in dual channel output mode.
$OUT1B^+$	42	Output	Serial data LVDS for channel 1 outputs positive B terminals. Works in two-track output mode.
$OUT1A^-$	43	Output	Serial data LVDS for channel 1 outputs A negative terminal.
$OUT1A^+$	44	Output	Serial data LVDS for channel 1 outputs A positive terminal.
SDO	46	Output	In serial programming mode (PAR/$\overline{SER}$ = 0V), SDO is the optional serial interface data output. The data on the SDO is read back from the mode control register and can be latched onto the falling edge of the SCK. The SDO is an open drain. NMOS output, requires an external 2k pull-up resistor to pull the level from 1.8V to 3.3V. If there is no need to read back from the mode control register, then the pull-up resistor is not necessary and the SDO can be left unconnected. In parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SDOA is an input responsible for enabling the internal 100Ω terminal resistor on the digital output. When used as an input, SDO can be driven using a 1.8V to 3.3V logic circuit via a 1k series resistor.
PAR/$\overline{SER}$	47	input	Programming Mode Select pins. Connect the pin to the ground to enable serial programming mode. $\overline{CS}$, SCK, SDI, SDO becomes a serial interface for controlling the ADC operation mode. Connecting the pin to V_{DD} enables parallel programming mode, where $\overline{CS}$,SCK, SDI, and SDO become parallel logic inputs for controlling a condensed set of ADC modes of operation.They should be PAR/$\overline{SER}$ connected directly to ground or device V_{DD} and must not be driven by a single logic signal.

V_{REF}	48	Output	Reference voltage output. Use a 1μF ceramic capacitor with a nominal voltage of 1.25V to bypass to ground.
SENSE	50	Input	Benchmark programming pin. Connecting the SENSE pin to V_{DD} will select the internal benchmark and a ±1V input range. Connecting SENSE pins to ground selects an internal reference and a ±0.5V input range. Applying an external reference between 0.625V and 1.3V to the SENSE pin will select an input range of ±0.8•$V_{SENSE.}$

Table 15

17. Package Description

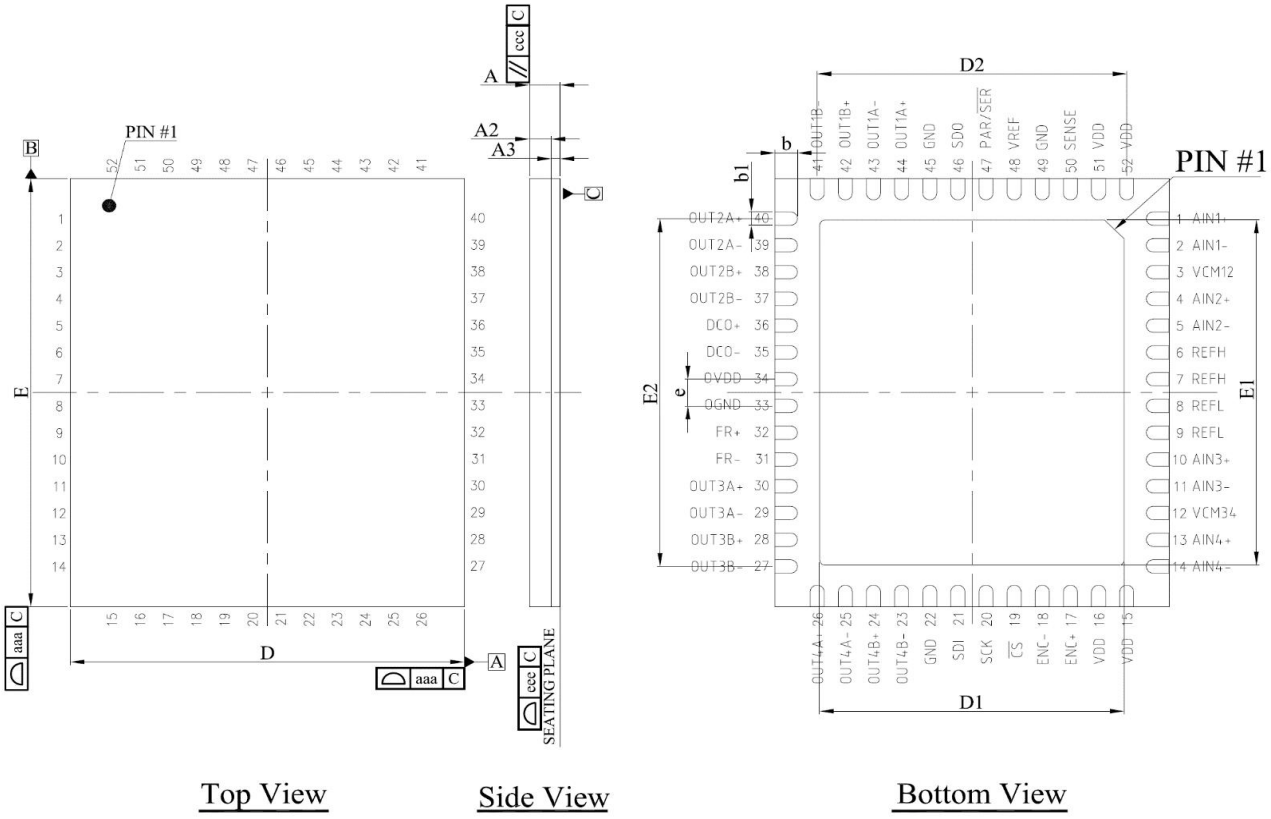


Figure 29

ITEM		Symbol	DIMENSION(mm)		
			MIN.	NOM.	MAX.
Total height		A	0.65	0.70	0.75
Mold thickness		A2	0.48	0.49	0.50
SBT thickness		A3	0.18	0.21	0.24
Lead length		b	0.30	0.40	0.50
Lead width		b1	0.20	0.25	0.30
Package size	X	D	6.90	7.00	7.10
	Y	E	7.90	8.00	8.10
E-pad size	X	D1	5.31	5.41	5.51
	Y	E1	6.35	6.45	6.55
Edge lead center to center	X	D2	5.45	5.50	5.55
	Y	E2	6.45	6.50	6.55
Lead pitch		e	0.5BSC		
Package profile of a surface		aaa	0.25		
Paralleliam		ccc	0.10		
Package profile of a surface		eee	0.10		

Table 16

18. Order Information

Model number	Package Description	Packaging form	MOQ
GX2170	52-Lead(7mm×8mm) LGA	Tray	490
GX2170K	52-Lead(7mm×8mm) LGA	Tray	490

19. Revision History

Editions	Dates	Description
0.1	2023/05	Draft, layout adjustments
0.1.1	2023/07	Update frequency range
1.0	2023/12	New packaging form & MOQ

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